ANALOG CIRCUITS

LECTURE NOTES

B.TECH
(II YEAR – II SEM)
(2020-21)

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MALLA REDDY COLLEGE
OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

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MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

II Year B.Tech. ECE-II Sem **L T/P/D C**
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(R20 A0405) ANALOG CIRCUITS

OBJECTIVE

The main objectives of the course are:

1. Study about Wave shaping concepts of both linear and non-linear circuits.
2. Study about the designing of multivibrators.
3. Study about Time Base Generator, understanding sampling gates and Logic Gates.
4 .Analysis of basic transistor amplifier circuits and their frequency response Characteristics, feedback amplifiers, oscillators, large signal amplifiers

UNIT – I BJT Amplifiers- Frequency Response: Frequency response of an amplifier, Analysis at low and High Frequencies, Hybrid-pi (π) common emitter transistor model, validity of hybrid- π model, variation of hybrid – π parameters, Millers theorem and its dual, the CE short circuit current gain, current gain with resistive load, gain-bandwidth product.

UNIT – II MULTISTAGE AMPLIFIERS: Distortion in amplifiers, Analysis of cascaded BJT amplifier, Darlington pair, Coupling schemes-RC coupled amplifier, transformer coupled amplifier, Direct coupled Amplifier.

UNIT - III LARGE SIGNAL AMPLIFIERS: Classification, Distortion in amplifiers, class A large signal amplifiers, efficiency of class A amplifier, class B power amplifier, efficiency of class B amplifier, class B push pull amplifier, Complementary symmetry class B push pull amplifiers, class AB push pull amplifier, Single tuned amplifier, Principles of Staggered tuning.

UNIT – IV MULTIVIBRATORS: Transistor as a switch, switching times of a transistor. Analysis of Bistable, Monostable and Astable Multivibrators, Schmitt trigger using transistors.

UNIT –V TIME BASE GENARATORS: General features of a Time Base Signal, Methods of Generating Time Base Wave forms, Basic Principles of Transistor Miller and Bootstrap Time Base Generator, Current Time Base Generator.

TEXT BOOKS:

1. Pulse, Digital and Switching Waveforms - J. Millman and H. Taub, McGraw-Hill, 1991.
2. Integrated Electronics-Jacob Millman and Christos C. Halkias,1991 Ed -2008,TMH.

REFERENCE BOOKS:

1. Pulse and Digital Circuits – A. Anand Kumar, PHI, 2005.
2. Pulse, Digital Circuits and Computer Fundamentals - R.Venkataraman.
3. Microelectric Circuits-Sedra and Smith-5 Ed., 2009, Oxford University press.
4. Electronic Circuit Analysis-K.LalKishore, 2004, BSP.

COURSE OUTCOMES:

At the end of the course, the student will be able to;

1. Understand the concepts of wave shaping circuits
2. Design of multivibrators for various applications,
3. Understand the concepts of Time Base Generators , sampling gates and logic gates
4. Analyzed the different types of amplifiers and oscillators

UNIT-I
BJT Amplifiers- Frequency Response

FREQUENCY RESPONSE OF AMPLIFIERS

For any electronic circuit, the behavior of amplifiers is affected by the frequency of the signal on their input terminal. This characteristic is known as the **frequency response**.

Frequency response is one of the most important property of amplifiers. In the frequency range that amplifiers have been designed for, they must deliver a constant and acceptable level of gain. The frequency response depends directly on the components and the architecture chosen for the design of the amplifier.

Before defining in details the frequency response, we need to present the unit of decibel (dB) and the logarithmic scale related to it. When studying the frequency response, it is indeed more suitable to convert either the power or voltage gain into dB and to represent the frequency scale in a logarithmic (log) scale.

If we consider an amplifier with power gain $\mathbf{A_P}$ and voltage gain $\mathbf{A_V}$, the power and voltage gain in dB are defined by:

$$A_P(dB) = 10\log(A_P)$$
$$A_V(dB) = 20\log(A_V)$$

While the gains in linear scale are always positive ($A_P, A_V \geq 0$), their equivalent in dB can either be positive if an amplification is being realized ($A_P, A_V > 1$) or negative if the input signal is attenuated ($A_P, A_V < 1$).

Often, it is not the gain $\mathbf{A_V(dB)}$ that is investigated but rather a normalized ratio $\mathbf{A_V/A_{V,mid}(dB)=20\log(A_V/A_{V,mid})}$. Where $A_{V,mid}$ is called the **midrange gain** and represents the maximum gain of the amplifier in its frequency working range, for example 20 Hz – 20 kHz for an audio amplifier.

Therefore, when $A_V=A_{V,mid}$, the normalized gain (written indifferently A_V) is $A_V(dB)=0$. This sets a 0 dB reference when the gain is maximum. It is important to note that when the power is divided by two, we observe that $\mathbf{A_P(dB)=10\log(0.5)=-3\ dB}$.

The frequency at which the power drops to 50 % of its midrange value is known as the **cutoff frequency** and noted $\mathbf{f_c}$. Each time that the power is halved, a reduction of 3 dB of the normalized gain is observed. Therefore $\mathbf{A_P=-3\ dB}$ corresponds to $\mathbf{A_{V,mid}/2}$, A_P=-6 dB corresponds to $A_{V,mid}/4$ and so on …

For this same frequency, the voltage (or current) is multiplied by a factor √2=0.7. Halving the voltage signal corresponds to a reduction of 6 dB and follows the same pattern as presented for the power gain.

The most common tool used to represent the frequency response of any system is the **Bode plot**. It consists of the normalized gain A_V(dB) as a function of the frequency in log scale. A simplified Bode graph of an amplifier is shown in the **Figure 1** below:

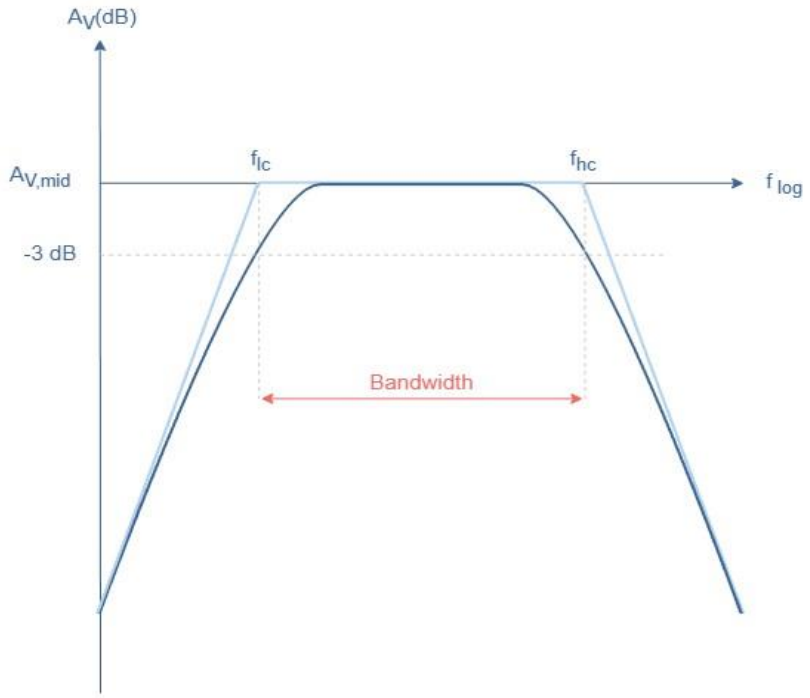


Fig 1 : Typical Bode graph of an amplifier

The light blue curve is called the asymptotic representation while the dark blue curve is the real frequency response of the circuit. In **Figure 1**, two different cutoff frequencies can be distinguished: $\mathbf{f_{lc}}$ for "low cutoff" and $\mathbf{f_{hc}}$ for "high cutoff". The quantity f_{hc}-f_{lc} is called the **bandwidth** and represents the frequency range where the gain is above the -3 dB.

EFFECT OF THE CAPACITORS:

Let us consider a Common Emitter Amplifier (CEA) which configuration is shown in **Figure 2.** The structure around the BJT transistor consists of a voltage divider network (R_1 and R_2), a load (R_L), coupling capacitors (C_1 and C_3) and a bypass capacitor C_2.

As capacitors have a property called **reactance** that is an equivalent of the resistance. The reactance (X_C) of capacitors depends on the frequency and the value of the capacitor, as in the below equation

$$X_C = \frac{1}{2\pi f C}$$

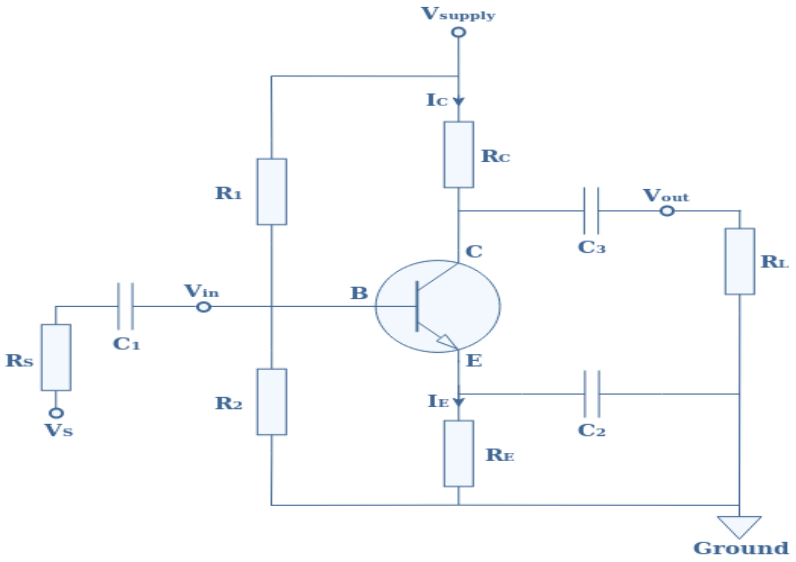


Fig 2: Common Emitter Amplifier

When the frequency is low, X_C tends to be high. Near DC signals, capacitors behave therefore as open circuits. On the other hand, when the frequency increases X_C tends to zero and capacitors act as short circuits.

At low input frequencies, the coupling capacitors will more likely block the signal, since X_{C1} and X_{C3} are higher, more voltage drop will be observed across C_1 and C_3. This results in a lower voltage gain.

At high input frequencies the bypass capacitor C_2 shortens the emitter branch to the ground and the voltage gain of the amplifier is $\mathbf{A_V=(R_C//R_L)/r_e}$ with r_e being the small diode emitter resistance. When the frequencies are lower, the resistance between the emitter and the ground is no longer only r_e but $\mathbf{R_E+r_e}$ and therefore the voltage gain decreases to $\mathbf{A_V=(R_C//R_L)/(R_E+r_e)}$.

There is another type of capacitors that affect the frequency response of the amplifier and is not represented in **Figure 2**. They are known as **internal transistor capacitors** and represented in **Figure 3** below :

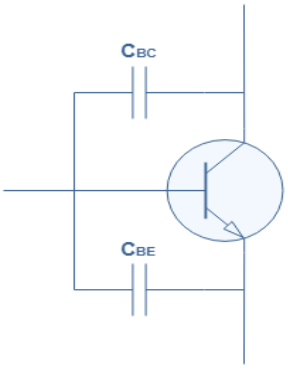


Fig 3: Internal transistor capacitors

Whereas the coupling and bypass capacitors act as **high-pass filter** (they block low frequencies), these internal capacitors behave differently. Indeed, if the frequency is low, C_{BC} and C_{BE} act as an open circuit and the transistor is not affected at all. However, if the frequency increases, more signal passes through them instead of going in the base branch of the transistor, therefore decreasing the voltage gain. The cutoff frequency of a RC filter:

$$f_c = \frac{1}{2\pi RC}$$

ANALYSIS AT LOW FREQUENCY

First of all we consider the input high-pass filter $R_{in}C_1$. Where R_{in} is the total input impedance of the amplifier which can be expressed as:

$$R_{in}=R_S+ (R_1//R_2//\beta R_E)$$

The low cutoff frequency of the input will therefore be:

$$f_{cl,in}=1/(2\pi R_{in}C_1)$$

The same procedure can be done for the output where the output resistance is

$$R_{out}=R_C//R_L$$

The low cutoff frequency of the output filter is:

$$f_{cl,out}=1/(2\pi R_{out}C_3)$$

Finally, for the bypass capacitor, the resistance formula is more complex and given by

$$R_{bypass}=R_E//((r_e+(R_S//\beta R_E)/\beta))$$

The low cutoff frequency of the bypass structure is thus:

$$f_{cl,bypass}=1/(2\pi R_{bypass}C_2)$$

One last thing we need to understand before plotting the Bode graph is about the slope out of the midrange values. The decrease of $A_{V,mid}$ with the frequency is called **roll-off** and its value for each simple RC filter is -20 dB/decade (dB/dec). This value means for high-pass filters (resp. low-pass filters) that each time the frequency is divided by 10 (resp. multiplied by 10), a decrease of -20 dB is observed for the gain of the amplifier.

When multiple filters are blocking the same range of frequencies, the roll-off is enhanced. In our example three filters are simultaneously blocking the frequencies below 35 Hz, the roll-off is therefore 3*(-20 dB/dec)=-60 dB/dec.

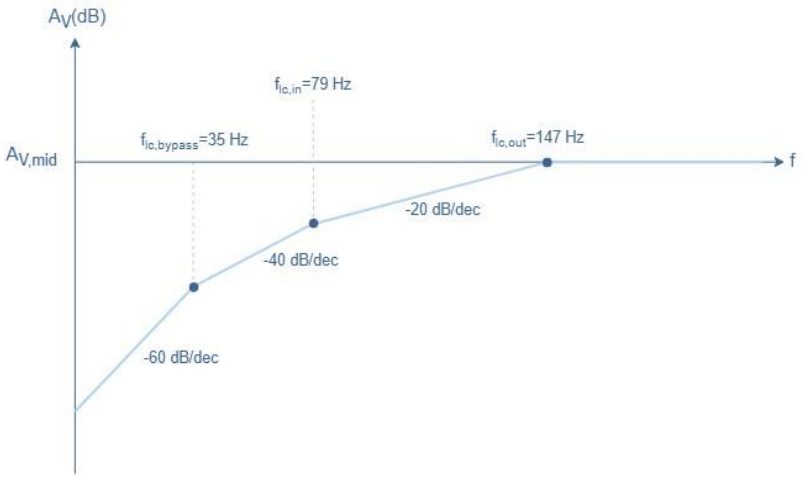


Fig 4 : Low frequency response of the CEA

ANALYSIS AT HIGH FREQUENCY

As stated previously, it is the internal transistor capacitors that will limit the gain at high frequencies acting as low-pass filters. It can be shown that the equivalent circuit of **Figure 2** at high frequency can be drawn such as presented in **Figure 5** :

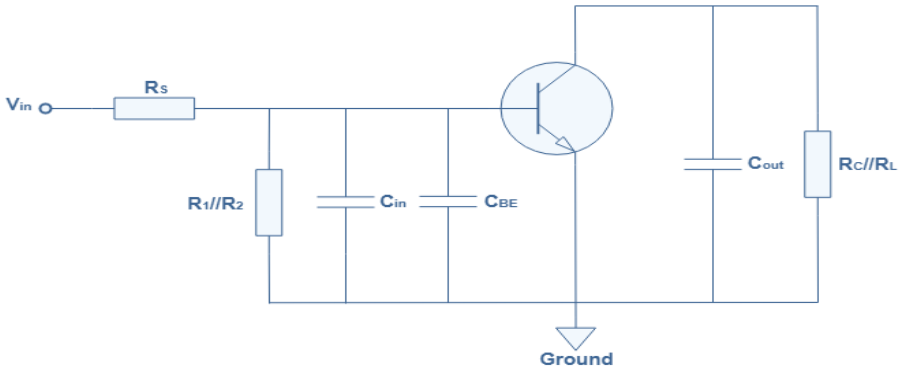


Fig 5 : Equivalent CEA at high frequency

We can note that the coupling capacitors are not represented since they behave as short circuits at high frequencies. Moreover, the emitter branch is shorten to the ground for the same reason applying to the bypass capacitor.

The internal capacitor C_{BC} is converted via **Miller's theorem** into the equivalent C_{in} and C_{out} capacitors. Moreover, this theorem states that

$$C_{in}=C_{BC}(A_{V,mid}+1) \text{ and}$$

$$C_{out}=C_{BC}(A_{V,mid}+1)/A_{V,mid}.$$

The total input capacitance of this circuit is

$$C_{IN}=C_{BE}+C_{in} ;$$

The total input resistance is

$$R_{IN}=R_S//R_1//R_2//\beta r_e.$$

The numerical application to our example gives

$A_{V,mid}=(R_C//R_L)/r_e=108$, $\mathbf{C_{IN}=575\ pF}$ and $\mathbf{R_{IN}=409\ \Omega.}$

The high cutoff frequency of the input is therefore

$$f_{hc,in}=1/(2\pi R_{IN}C_{IN})=677\ kHz.$$

From the output point of view, the high cutoff frequency is simply given by the filter $(R_C//R_L)C_{out}$ with $\mathbf{C_{out}=5.3\ pF}$: $\mathbf{f_{hc,out}=1/(2\pi(R_C//R_L)C_{out})=1.1\ MHz}$.

The information given here is summarized in a Bode plot representing the high frequency response of the CEA in asymptotic representation:

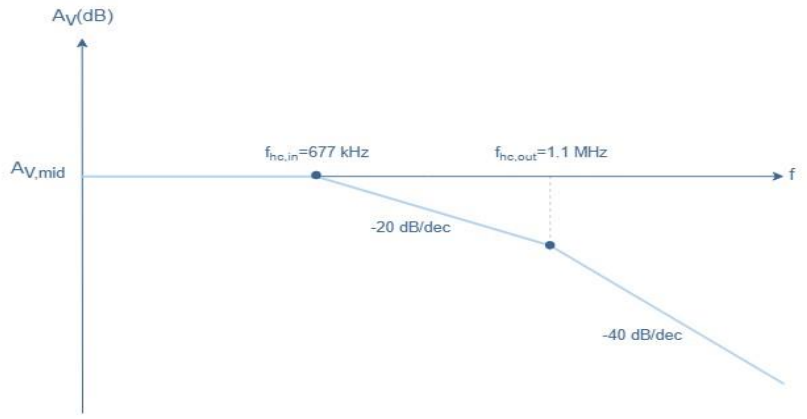


Fig 6: High frequency response of the CEA

By merging the two Bode graphs obtained for the low and high frequency responses in **Figure 4 and 6**, we can now plot the overall frequency response of the CEA configuration

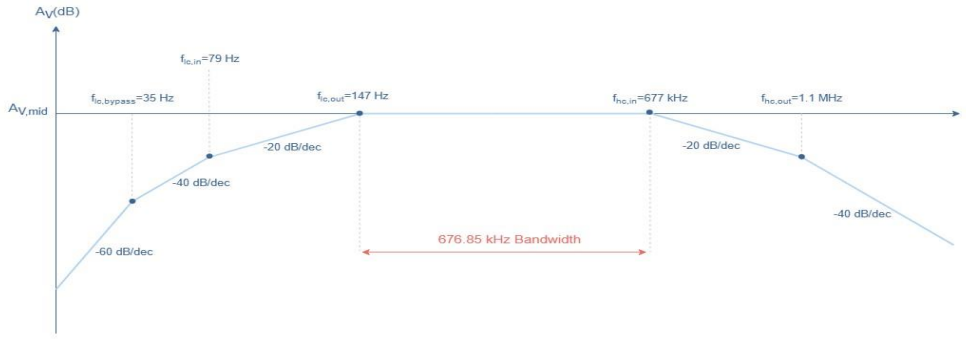


Fig 7: Total frequency response of the CEA

Hybrid-pi (π) common emitter transistor model

For *amplifier circuits Common Emitter configuration is preferred* Because for Common Collector (hrc < 1). For Common Collector Configuration, voltage gain Av < 1. So even by cascading you can't increase voltage gain. For Common Base, current gain hib < 1. So overall voltage gain is < 1. But for Common Emitter, hre» 1. Therefore Voltage gain can be increased by cascading Common Emitter stage. So Common Emitter configuration is widely used.

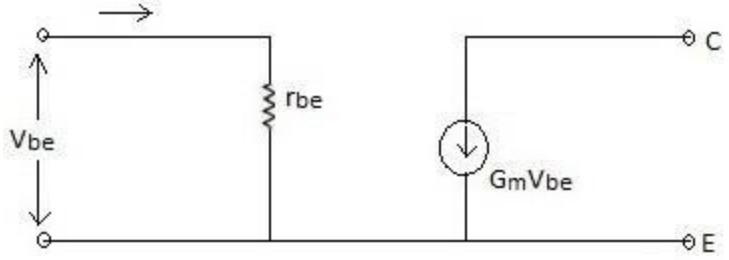
Under reverse bias condition the capacitance at the junction is called transition or space charge capacitance. Under forward bias condition the capacitance is called diffusion or storage capacitance. At high frequencies, BJT cannot be analysed by h-parameters.

Giacolleto model - hybrid π equivalent circuit

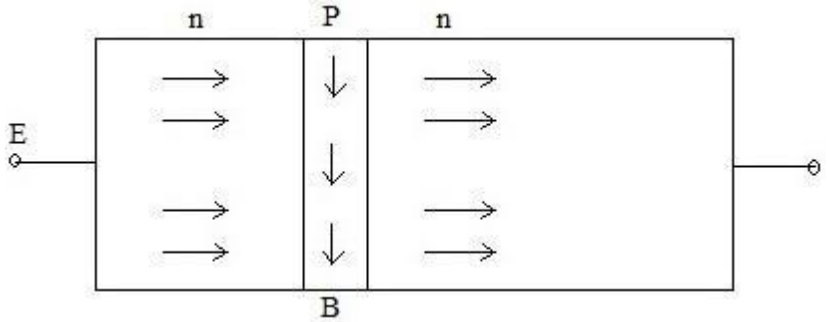
Desirable features of hybrid π equivalent circuit are:
(1) The value of components in the equivalent circuit are independent of frequencies.
(2) The values of all the resistive components in the equivalent circuit can be determined from the known or Specified values of h-parameters at low frequencies.
(3) The results obtained by using this equivalent circuit agrees with the experimental result.

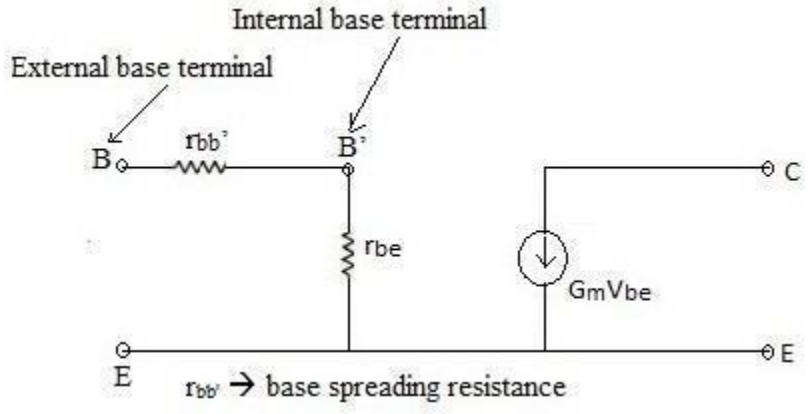
The components of the equivalent circuit exist in the form of π hence the name.

For small signal behaviour the transistor at its input port behaves as a resistor.

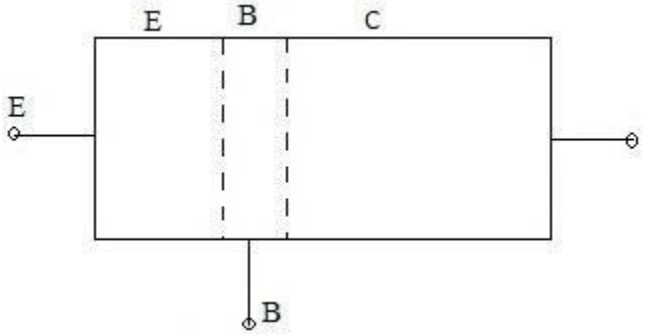


The output port is a dependent current source.

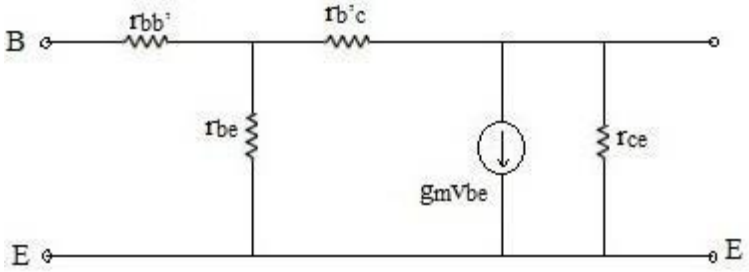




Because the base (B) is lightly doped all the depletion region lies entirely in the Base region. So, when the collector voltage is increased the depletion region in the base increases.



rce --> This resistance is added to compensate for the change in IC due to change in VCE.



The *Hybrid-π* or *Giacoletto Model* for the Common Emitter amplifier circuit (single stage) is as shown :

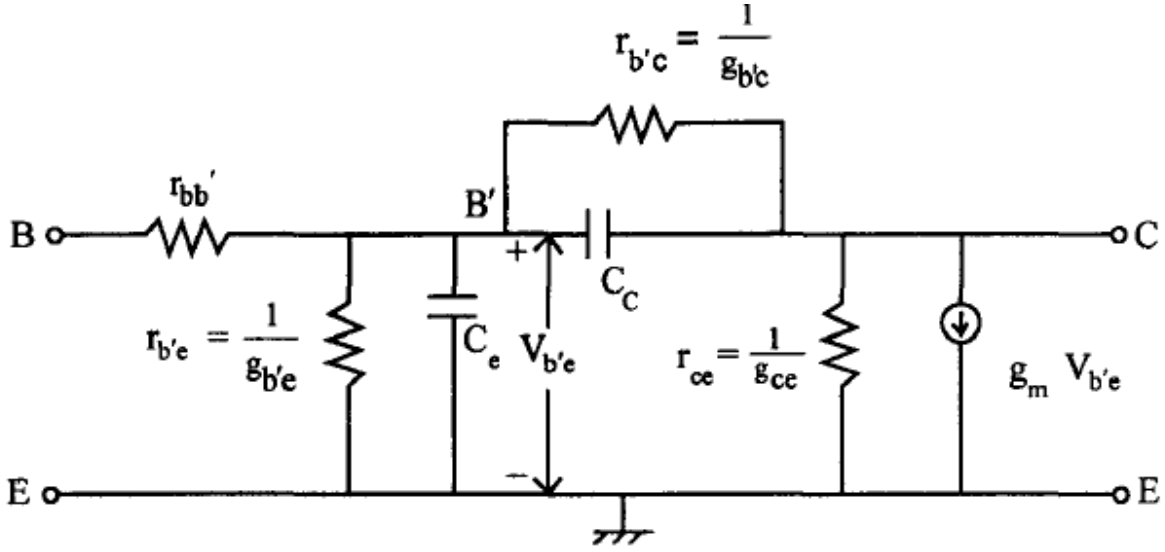


Fig 8 : Hybrid-π CE BJT Model

Analysis of this circuit gives satisfactory results at *all* frequencies not only at *high frequencies* but also at *low frequencies.* All the parameters are assumed to be independent of frequency.

Circuit Components

B' is the internal node of the base of the Transconductance amplifier. It is not physically accessible.
The base spreading resistance rb'b is represented as a *lumped* parameter between base B and internal node B'. ($g_m\ V_{b'e}$) is a current generator. Vb'e is the input voltage across the emitter junction. If $V_{b'e}$ increases, more carriers are injected into the base of the transistor. So the increase in the number of carriers is α $V_{b'e}$). This results in small signal current (since we are taking into account changes in $V_{b'e}$). This effect is represented by the current generator $g_m\ V_{b'e}$. This represents the current that results because of changes in $V_{b'e}$ when C is shorted to E.

When the number of carriers injected into the base increase, base recombination also increases. So this effect is taken care of by$g_{b'e}$. As recombination increases, base current increases. Minority carrier storage in the *base is* represented by c_e the diffusion capacitance.

According to Early Effect, the change in voltage between Collector and Emitter changes the base width. So base width will be modulated according to the voltage between Collector and Emitter. When base width changes, the minority carrier concentration in base changes. Hence the current which is proportional to carrier concentration also changes. So I_E changes and hence I_C changes. This feedback effect [I_E on input side, I_C on output side] is taken into account by connecting $g_{b'c}$ between B', and C. The conductance between Collector and
Base isg_{ce}. C_c represents the collector junction barrier capacitance.

The High frequency model parameters of a BJT in terms of low frequency hybrid parameters is given below

- Tran conductance $g_m = I_C/V_T$
- Internal Base node to emitter resistance $r_{b'e} = h_{fe}/\ g_m = (h_{fe}*V_T\ )/\ I_C$
- Internal Base node to collector resistance $r_{b'c}$ = ($h_{re}*\ r_{b'e}$) / (1-h_{re}) assuming hre << 1 it reduces to $r_{b'c}$ = ($h_{re}*\ r_{b'e}$)
- Base spreading resistance $r_{bb'} = h_{ie} - r_{b'e}$ = h_{ie} – (h_{fe}* Vt)/ Ic
- Collector to emitter resistance r_{ce} = 1 / (h_{oe} – (1+ h_{fe})/ $r_{b'c}$)

Variation of Hybrid Parameters with $|I_C|$, $|V_{CE}|$and T

1) **Transconductance Amplifier or Mutual Conductance (gm):**

$g_m = I_C/V_T$

g_m is α I_C

V_T = T/ll,600

Therefore g_m α 1/T

g_m is independent of V_{CE}
Since in the active region of the transconductance, Ic is independent of V_{CE}

2) Base Emitter Resistance (r b'e)

$r_{b'e} = h_{fe}/ g_m = (h_{fe}*V_T)/ I_C$

Therefore $r_{b'e}$ α $\frac{1}{I_C}$

$r_{b'e}$ increases as T increases since $r_{b'e}$ α V_T.

3) Base Spread Resistance ($r_{bb'}$)

$r_{bb'}$ decreases with increase in I_C

Since as I_C increases, conductivity increases. So $r_{bb'}$ decreases, because of conductivity modulation. But $r_{bb'}$ increases with increase in Temperature. Because as T increases, mobility of the carriers decreases. So conductivity decreases. So $r_{bb'}$ increases.

Miller's Theorem

Fig. 9(a) shows an amplifier with a capacitor between input and output terminals. It is called as feedback capacitor. When the gain K is large, the feedback will change the input Z and output Z of the circuit.

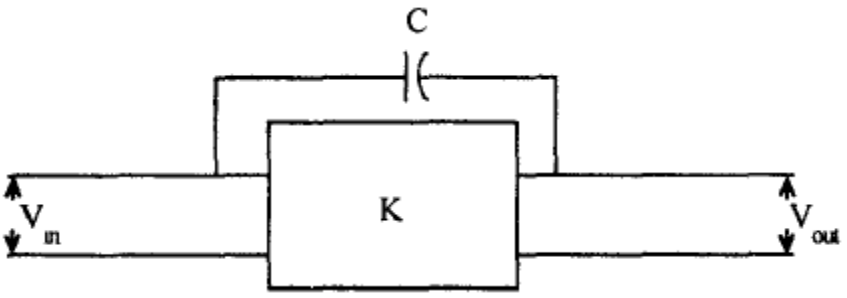


Fig. 9 (a) Feedback Capacitor

A circuit as shown above is difficult to analyze, because of capacitor. So according to the Miller's theorem, the feedback capacitor can be split into two values, one as connected in the input side and the other on the output side, as shown in Fig. 9 (b).

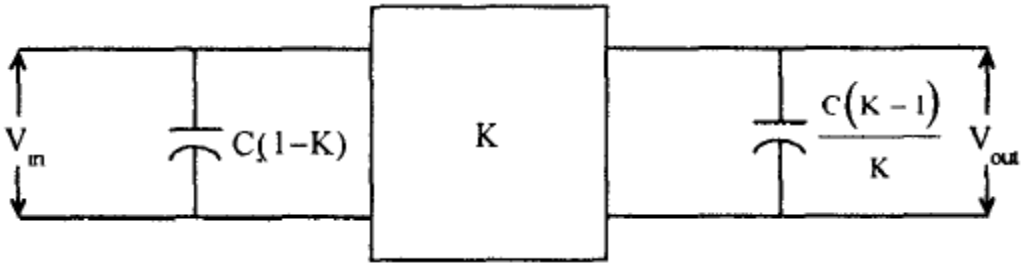


Fig. 9 (b) Splitting of feedback capacitor using Miller's Theorem

Mathematical Proof of Miller's Theorem:

The AC current passing through capacitor (C) in Fig. 9 (a) is

$$I_C = \frac{V_{in}-V_{out}}{\left(\frac{1}{jwC}\right)} = \frac{(V_{in}-V_{out})}{-jX_C}$$

$$V_{out} = \mathrm{K}\, V_{in}$$

Therefore $I_C = \frac{(V_{in} - \mathrm{K}\, V_{in})}{-jX_C} = \frac{V_{in}(1-\mathrm{K})}{-jX_C}$

$$\frac{V_{in}}{I_C} = Z_{in} = \frac{V_{in}}{\frac{V_{in}(1-\mathrm{K})}{-jX_C}} = \frac{-jX_C}{(1-\mathrm{K})}$$

$$= \frac{-j}{2\pi f C(1-\mathrm{K})} \qquad \text{since } X_C = \frac{1}{2\pi f C}$$

$\frac{V_{in}}{I_C}$ is the input Z as seen from the input terminals.

Therefore $Z_{in} = \frac{-j}{2\pi f[C(1-\mathrm{K})]}$

Therefore $C_{in} = \mathrm{C}\,(1\text{-}\mathrm{K})$

Similarly output capacitance can be derived as follows:

Current in the capacitor,

$$I_C = \frac{V_{out} - V_{in}}{-jX_C} = \frac{V_{out}(1 - \frac{V_{in}}{V_{out}})}{-jX_C}$$

$$I_C = \frac{V_{out}(1 - \frac{1}{K})}{-jX_C}$$

Rearranging the terms we get ,

$$Z_{out} = \frac{-jX_C}{(1 - \frac{1}{K})} = \frac{-jX_C}{(\frac{K-1}{K})} \qquad \text{since } Z_{out} = \frac{V_{out}}{I_C}$$

$$= \frac{-j}{2\pi f C(\frac{K-1}{K})}$$

Therefore C_{out} (Miller) = $\mathrm{C}\,(\frac{K-1}{K})$

Miller's Theorem

It states that if an impedance Z is connected between the input and output terminals, of a network, between which there is voltage gain, K, the same effect can be had by removing Z and connecting an impedance Z_i at the input = $\frac{Z}{(1-K)}$ and Z_o across the output = $\frac{ZK}{(\mathrm{K}-\mathrm{I})}$.

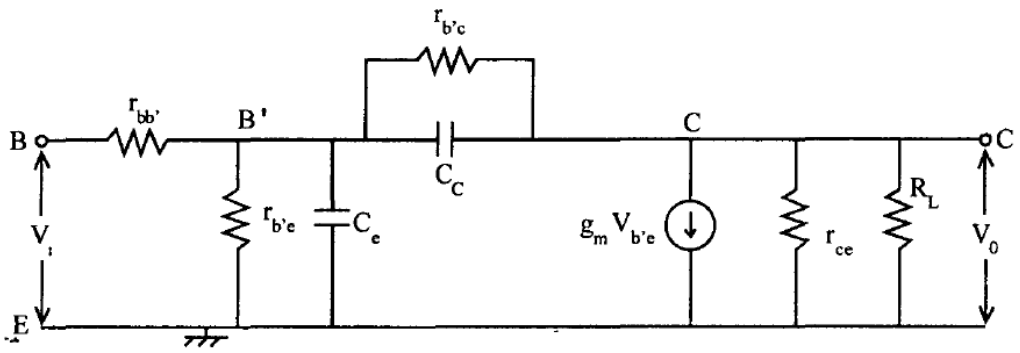


Fig 10: High Frequency equivalent circuit with resistive load

$$C_{bFC} = C_c$$

$r_{b'c}$ and $C_{b'c}$ are between the input termed B' and output termed C. The voltage gain of the amplifier = $\frac{V_{Ce}}{V_{b'e}}$ = K (> > 1). Therefore by Miller's theorem, C_c and $r_{b'c}$ can be connected between B' and E (input side) with values = $\frac{C_c}{1-k}$ and $r_{b'c}.K$ (1 - K) respectively. On the output side between Collector and emitter as $C_c \frac{(K-1)}{K}$ and $\frac{(K-1)}{}$ resting.

Therefore high frequency equivalent circuit using Miller's theorem reduces to, (neglecting rbb ,)

$$K = \frac{V_{Ce}}{V_{b'e}}$$

V_{Ce}= -$I_C.R_L$., Negative is used since current direction is opposite

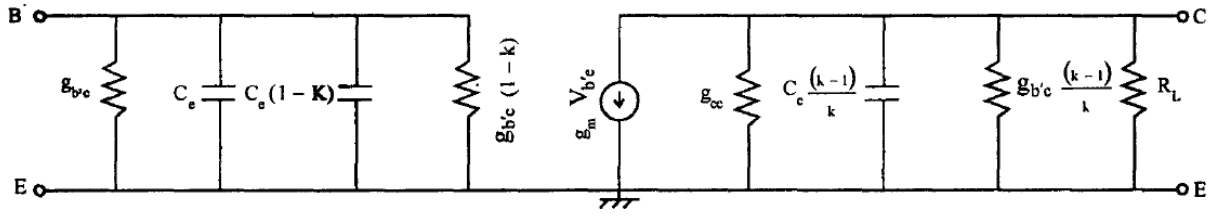


Fig 11 : Circuit after applying Millers Theorem

$$K = \frac{-I_C.R_L}{V_{b'e}}$$

But $\frac{I_C}{V_{b'e}} = g_m$

Therefore K = -g_m . R_L

The CE Short Circuit Current gain (Ai)

This is the circuit of transistor amplifier in common emitter configuration

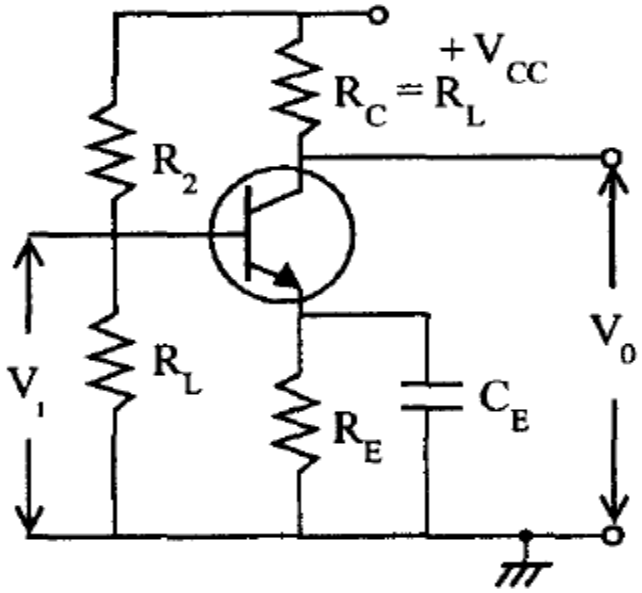


Fig.12 CE Amplifier Circuit

The approximate equivalent circuit at high frequencies, with output shorted is

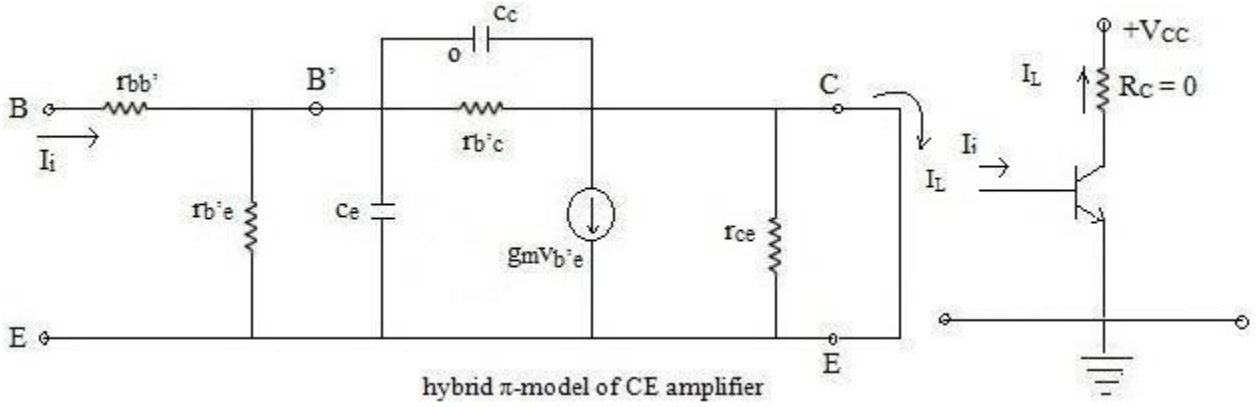


Fig.13 Simplified equivalent circuit

r_{b^Fe} is assumed to be very large. So it is open circuit.
r_{ce} disappears since it is in shunt with short circuited output.

$$I_L = -g_m V_{b^Fe}$$

Negative sign taking the direction of current into acount. $I_L$is contributed by the current source only.

$$V_{b^Fe} = I \times Z = I \times \frac{1}{Y}$$

$$V_{b^Fe} = \frac{I_i X 1}{g_{b^Fe} + j\omega C_e}$$

Therefore $I_L = \frac{-g_m I_i}{g_{b'e} + j\omega C_e}$

Conductances in parallel get added

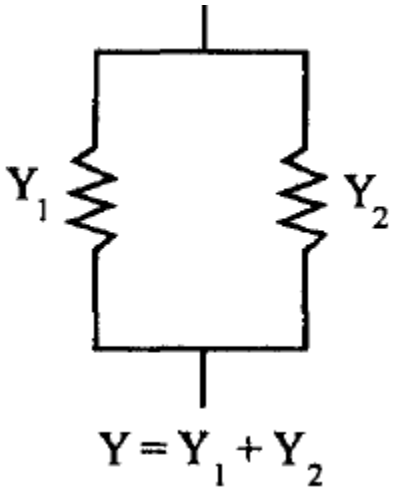


Fig.14 Conductances in parallel

Therefore current gain under short circuit conditions is,

$$A_i = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega C_e}$$

But $g_{b'e} = \frac{g_m}{h_{fe}}$

$C_e = \frac{g_m}{2\pi f_T}$

Therefore by substituting all these terms in the above equation, we get

$$A_i = \frac{I_L}{I_i} = \frac{-g_m}{\frac{g_m}{h_{fe}} + \frac{j\omega g_m}{2\pi f_T}}$$

$$= \frac{-1}{\frac{1}{h_{fe}} + \frac{j2\pi f}{2\pi f_T}} = \frac{-h_{fe}}{1 + \frac{jh_{fe} \cdot f}{f_T}}$$

Since $\frac{f_T}{h_{fe}} = f_\beta$

Therefore $A_i = \frac{-h_{fe}}{1 + j(\frac{f}{f_\beta})}$

When $f = f_\beta$, A_i falls by $\frac{1}{\sqrt{2}}$, or by 3db. The frequency range f_β is called Bandwidth of the amplifiers.

f_β: Is the frequency at which the short circuit gain in common emitter configuration falls by 3 db.

f_T: This is defined as the frequency at which the common emitter shunt circuit current gain becomes 1.

Let $f = f_T$, $A_i = 1$

Therefore $1 = \frac{h_{fe}}{\sqrt{1+(\frac{f_T}{f_\beta})^2}}$

$$1 + (\frac{f_T}{f_\beta})^2 = h_{fe}^2$$

$$(\frac{f_T}{f_\beta})^2 = h_{fe}^2 - 1 = h_{fe}^2 \qquad \text{since } h_{fe} >> 1$$

Therefore $f_T = f_\beta . h_{fe}$

Where f_β - is the Bandwidth of the transistor

h_{fe} - is the current gain

f_T - is the current gain, Bandwidth product

In Common Emitter configurations, $A_i >> 1$. But as frequency increases A_i decreases. f_T depends on the operating point of the transistor. The graph of f_T versus I_C for a transistor is as shown,

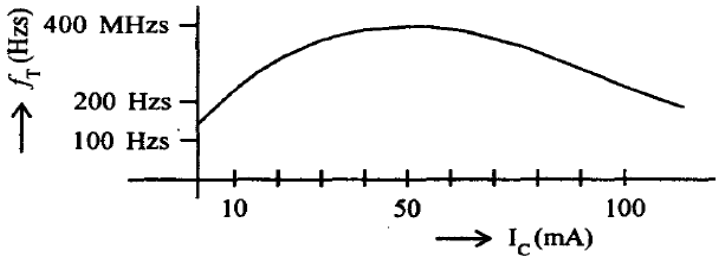


Fig.15 Variation of I_C with frequency

For a typical transistor, f_T = 80 MHz

f_β = 1.6 MHz

Current gain with resistive load

$$f_T = f_\beta . h_{fe} = \frac{g_m}{2\pi(C_e + C_c)}$$

Considering the load resistance R_L,

$V_{b'e}$ is the input voltage and is equal to V_1

V_{Ce} is the output voltage and is equal to V_2

$$K_2 = \frac{V_{Ce}}{V_{b'e}}$$

The equivalent circuit is as shown below:

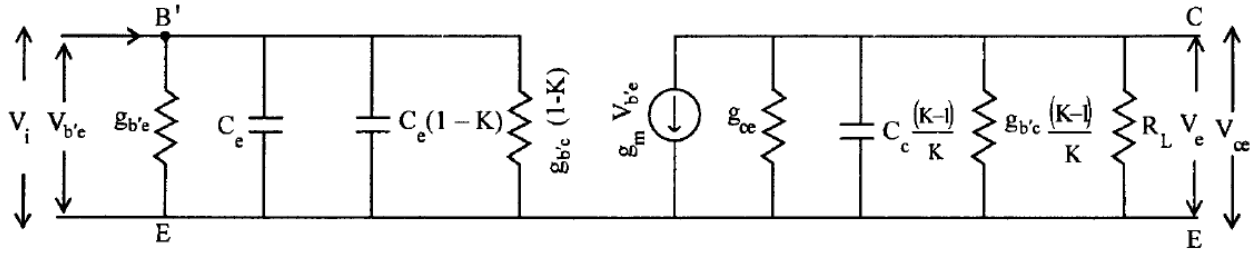


Fig.16 Equivalent circuit taking Load resistance into account

This circuit is still complicated for analysis.

Because, there are two time constants associated with the input and the other associated with the output. The output time constant will be much smaller than the input time constant. So it can be neglected.

K = Voltage gain. It will be >> 1

Therefore $g_{b'c}\left(\frac{K-1}{K}\right) = g_{b'c}$

$g_{b'c} < g_{Ce}$ since $r_{b'c}$ = 4 MΩ, r_{Ce} = 80 K (typical values)

So $g_{b'c}$ can be neglected in the equivalent circuit.

In a wide band amplifier R_L will not exceed 2KΩ, since $f_H \propto \frac{1}{R_L}$. If R_L is small, f_H is large.

$$f_H = \frac{1}{2\pi C_S (R_C \| R_L)}$$

Therefore g_{Ce} can be neglected compared with R_L.

Therefore the output circuit consists of current generator $g_m V_{b'e}$ feeding the load R_L so the Circuit simplifies as shown in Fig. 17

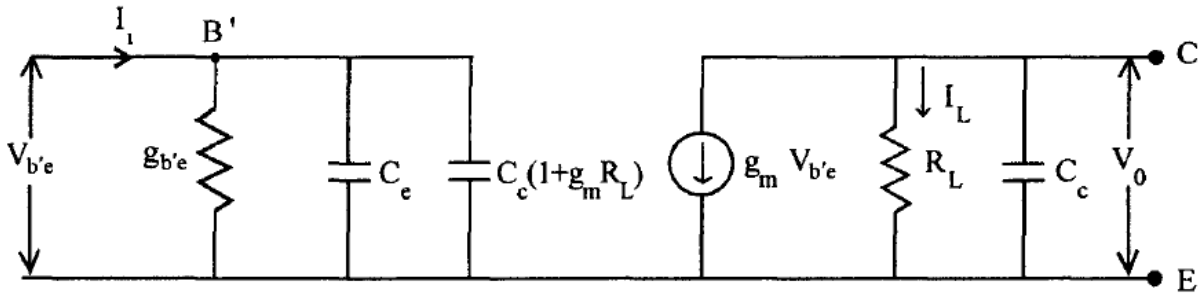


Fig.17 Simplified equivalent circuit

K = $\frac{V_{Ce}}{V_{bFe}}$ = $-g_m R_L$; g_m = 50 mA\V, R_L =2KΩ (typical values)

K = -100

So the maximum value is g_{bFc} (1-K) = 0.02595. So this can be neglected compared to g_{bFe}= 1mA\V.

R_L Should not exceed 2KΩ, therefore if R_L > 2KΩ, $C_C(1 + g_m R_L)$ becomes very large and so band pass becomes very small.

$C_C\left(\frac{K-1}{K}\right) = C_C$

When R_L = 2KΩ,

The output time constant is,

$R_L . C_C$= 2 x 10^3 x 3 x 10^{-12} = 6 x 10^{-9} s (typical value)

Input time constant is,

$r_{bFe}\,[C_e + C_C[1 + g_m R_L\,]]$ = 403 x 10^{-6} s

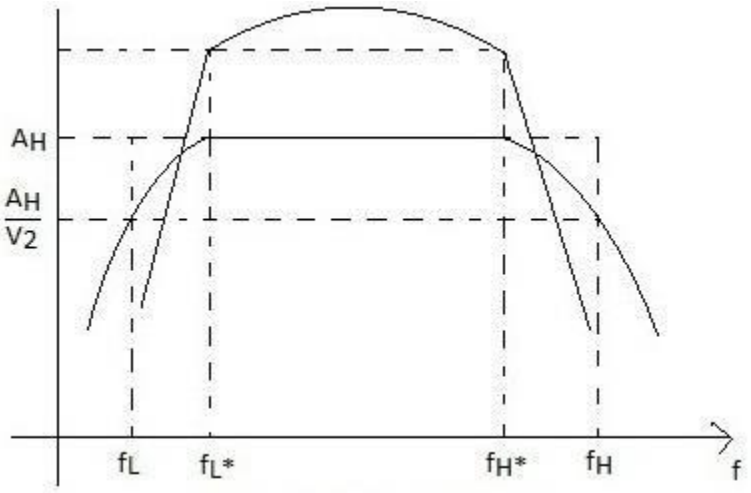
So the band pass of the amplifier will be determined by the time constant of the input circuit.

The 3db frequency $f_M = \frac{1}{2\pi r_{bFe} C} = \frac{g_{bFe}}{2\pi C}$

Where C = $[C_e + C_C[1 + g_m R_L\,]]$

Bandwidth of a multistage amplifier

The range of frequencies which are amplified without much variation in gain is called bandwidth of amplifiers. Human ears are insensitive to the variation of power gain of about 3dB. Hence, frequency range from lower 3dB to upper 3dB is considered as bandwidth of single stage amplifier. Bandwidth of single stage amplifier.



Amplifier response of an amplifier

Bandwidth (BW) = fH – fL ~ fH

Lower 3dB frequency of multistage amplifier

The lower 3db frequency of n identical cascaded stages as f_L(n).It is the frequency for which the overall gain falls to $\frac{1}{\sqrt{2}}$ (3 db) of its midband value.

$$\frac{1}{\sqrt{1+\left[\frac{f_L}{f_{L(n)}}\right]^2}}^{n} = \frac{1}{\sqrt{2}}$$

$$\left[\sqrt{1+\left[\frac{f_L}{f_{L(n)}}\right]^2}\right]^{n} = \sqrt{2}$$

Squaring on both sides we get

$$\left[1+\left[\frac{f_L}{f_{L(n)}}\right]^2\right]^{n} = 2$$

Taking nth root on both sides

$$1+\left[\frac{f_L}{f_{L(n)}}\right]^2 = 2^{\frac{1}{n}}$$

$$\left[\frac{f_L}{f_{L(n)}}\right]^2 = 2^{\frac{1}{n}} - 1$$

Taking square root on both sides

$$\left[\frac{f_L}{f_L(\mathrm{n})}\right] = \sqrt{2^{\frac{1}{n}} - 1}$$

$$f_L(\mathrm{n}) = \frac{f_L}{\sqrt{2^{\frac{1}{n}} - 1}}$$

Higher 3dB frequency of multistage amplifier

The higher 3db frequency of n identical cascaded stages as f_H(n). It is the frequency for which the overall gain falls to $\frac{1}{\sqrt{2}}$ (3 db) of its midband value.

$$\left[\frac{1}{\sqrt{1+\left[\frac{f_H(\mathrm{n})}{f_H}\right]^2}}\right]^n = \frac{1}{\sqrt{2}}$$

$$\left[\sqrt{1 + \left[\frac{f_H(\mathrm{n})}{f_H}\right]^2}\right]^n = \sqrt{2}$$

Squaring on both sides we get

$$\left[1 + \frac{f_H(\mathrm{n})^2}{f_H}\right]^n = 2$$

Taking nth root on both sides

$$1 + \left[\frac{f_H(\mathrm{n})}{f_H}\right]^2 = 2^{\frac{1}{n}}$$

$$\left[\frac{f_H(\mathrm{n})}{f_H}\right]^2 = 2^{\frac{1}{n}} - 1$$

Taking square root on both sides

$$\left[\frac{f_H(\mathrm{n})}{f_H}\right] = \sqrt{2^{\frac{1}{n}} - 1}$$

$$f_H(\mathrm{n}) = f_H\sqrt{2^{\frac{1}{n}} - 1}$$

UNIT-II
Multi-stage amplifiers

In practical applications, the output of a single state amplifier is usually insufficient, though it is a voltage or power amplifier. Hence they are replaced by **Multi-stage transistor amplifiers**.

In Multi-stage amplifiers, the output of first stage is coupled to the input of next stage using a coupling device. These coupling devices can usually be a capacitor or a transformer. This process of joining two amplifier stages using a coupling device can be called as **Cascading**.

The following figure shows a two-stage amplifier connected in cascade.

The overall gain is the product of voltage gain of individual stages.

$$A_V = A_{V1} \times A_{V2} = \frac{V_2}{V_1} \times \frac{V_o}{V_2} = \frac{V_o}{V_1}$$

Where A_V = Overall gain,

A_{V1} = Voltage gain of 1st stage, and

A_{V2}= Voltage gain of 2nd stage.

If there is n number of stages, the product of voltage gains of those **n** stages will be the overall gain of that multistage amplifier circuit.

Purpose of coupling device

The basic purposes of a coupling device are

- To transfer the AC from the output of one stage to the input of next stage.
- To block the DC to pass from the output of one stage to the input of next stage, which means to isolate the DC conditions.

Types of Coupling

Joining one amplifier stage with the other in cascade, using coupling devices form a **Multi-stage amplifier circuit**. There are **four** basic methods of coupling, using these coupling devices such as resistors, capacitors, transformers etc. Let us have an idea about them.

Resistance-Capacitance Coupling

This is the mostly used method of coupling, formed using simple **resistor- capacitor** combination. The capacitor which allows AC and blocks DC is the main coupling element used here.

The coupling capacitor passes the AC from the output of one stage to the input of its next stage. While blocking the DC components from DC bias voltages to effect the next stage. Let us get into the details of this method of coupling in the coming chapters.

Impedance Coupling

The coupling network that uses **inductance** and **capacitance** as coupling elements can be called as Impedance coupling network. In this impedance coupling method, the impedance of coupling coil depends on its inductance and signal frequency which is **jwL**. This method is not so popular and is seldom employed.

Transformer Coupling

The coupling method that uses a **transformer as the coupling** device can be called as Transformer coupling. There is no capacitor used in this method of coupling because the transformer itself conveys the AC component directly to the base of second stage.

The secondary winding of the transformer provides a base return path and hence there is no need of base resistance. This coupling is popular for its efficiency and its impedance matching and hence it is mostly used.

Direct Coupling

If the previous amplifier stage is connected to the next amplifier stage directly, it is called as **direct coupling**. The individual amplifier stage bias conditions are so designed that the stages can be directly connected without DC isolation.

The direct coupling method is mostly used when the load is connected in series, with the output terminal of the active circuit element. For example, head-phones, loud speakers etc.

Role of Capacitors in Amplifiers

Other than the coupling purpose, there are other purposes for which few capacitors are especially employed in amplifiers. To understand this, let us know about the role of capacitors in Amplifiers.

The Input Capacitor C_{in}

The input capacitor C_{in} present at the initial stage of the amplifier, couples AC signal to the base of the transistor. This capacitor C_{in} if not present, the signal source will be in parallel to resistor R_2 and the bias voltage of the transistor base will bechanged.

Hence C_{in} allows, the AC signal from source to flow into input circuit, without affecting the bias conditions.

The Emitter By-pass Capacitor Ce

The emitter by-pass capacitor C_e is connected in parallel to the emitter resistor. It offers a low reactance path to the amplified AC signal.

In the absence of this capacitor, the voltage developed across R_E will feedback to the input side thereby reducing the output voltage. Thus in the presence of C_e the amplified AC will pass through this.

Coupling Capacitor CC

The capacitor C_C is the coupling capacitor that connects two stages and prevents DC interference between the stages and controls the operating point from shifting. This is also called as **blocking capacitor** because it does not allow the DC voltage to pass through it.

In the absence of this capacitor, R_C will come in parallel with the resistance R_1 of the biasing network of the next stage and thereby changing the biasing conditions of the next stage.

Amplifier Consideration

For an amplifier circuit, the overall gain of the amplifier is an important consideration. To achieve maximum voltage gain, let us find the most suitable transistor configuration for cascading.

CC Amplifier

- Its voltage gain is less than unity.
- It is not suitable for intermediate stages.

CB Amplifier

- Its voltage gain is less than unity.
- Hence not suitable for cascading.

CE Amplifier

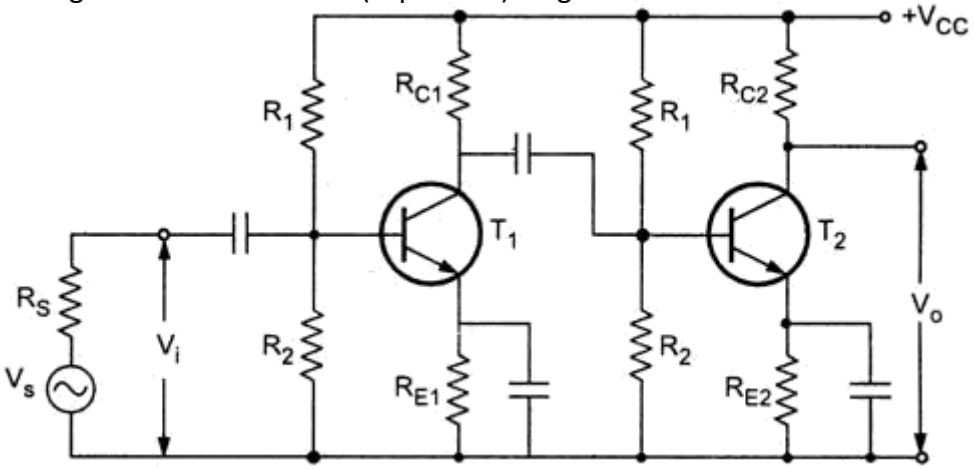
- Its voltage gain is greater than unity.
- Voltage gain is further increased by cascading.

The characteristics of CE amplifier are such that, this configuration is very suitable for cascading in amplifier circuits. Hence most of the amplifier circuits use CE configuration.

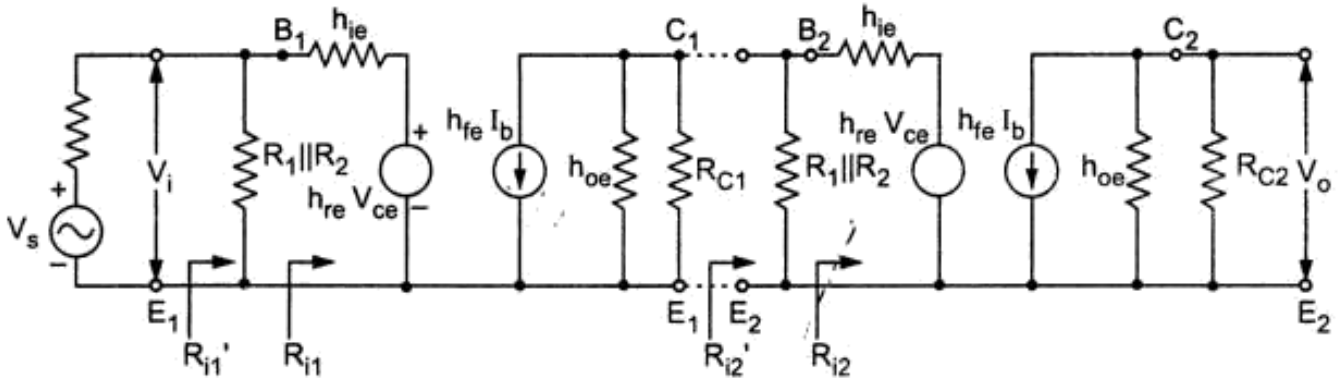
Two Stage CE-CE Cascade Amplifier

The impact of input and output loading can be minimized by cascading two amplifiers with appropriate input and output characteristics. Multistage cascading can be used to create amplifiers with high input resistance, low output resistance and large gains.

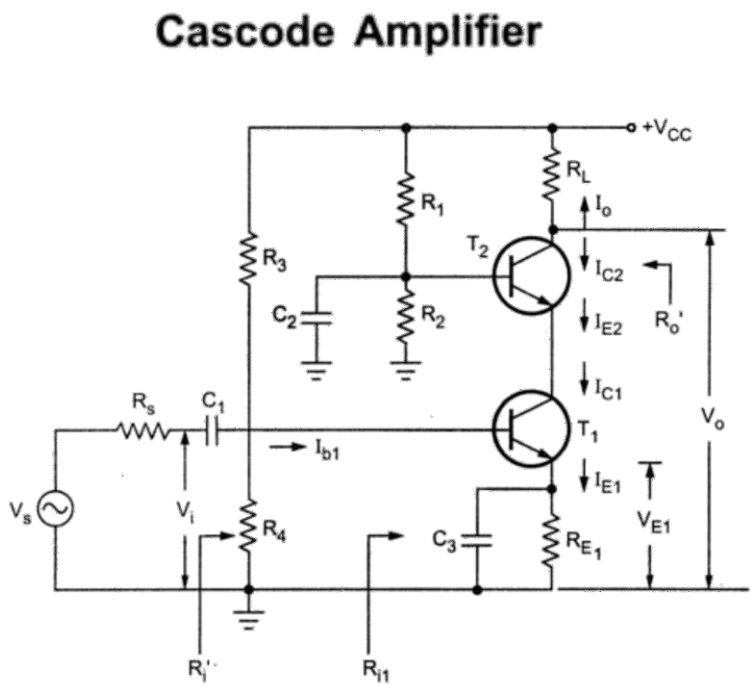
The complication in calculating the gain of cascaded stages comes from the non-ideal coupling between stages due to loading. Two cascaded common emitter stages are shown in below figure. Because the input resistance of the second stage (resistors R_1 and R_2) forms a voltage divider with the output resistance (R_{C1}) of the first stage, the total gain is not simply the product of the gain for the individual (separated) stages.



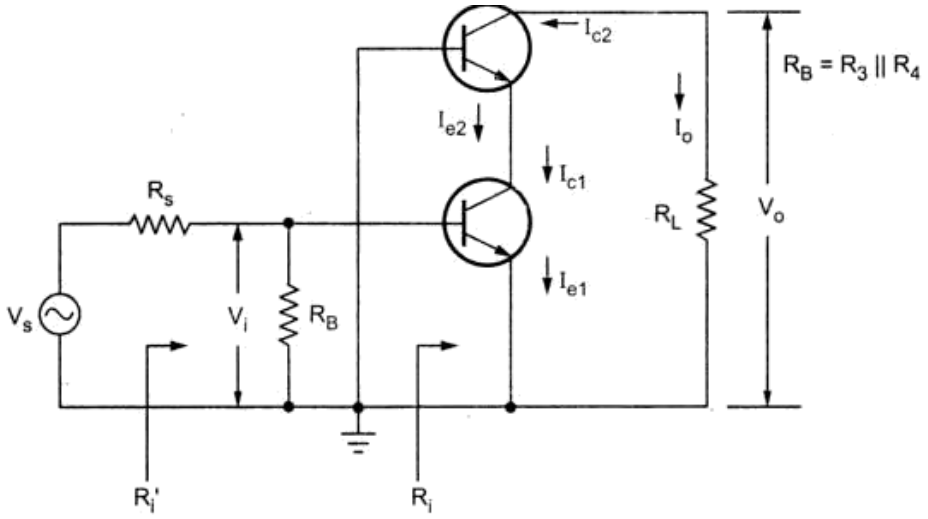
h-parameter equivalent circuit



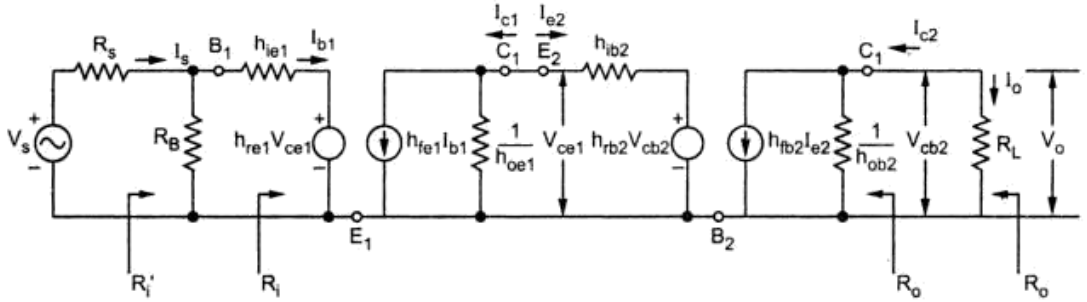
Cascode Amplifier



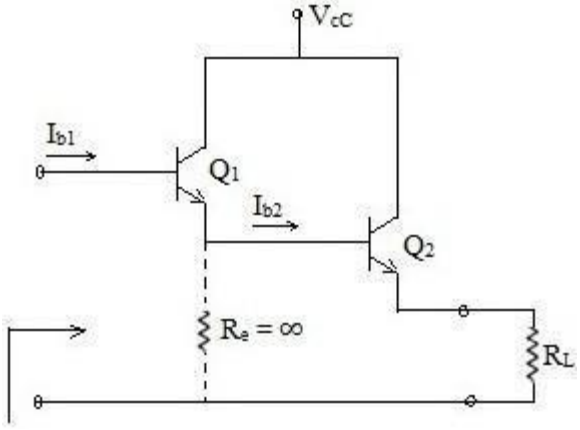
AC equivalent circuit



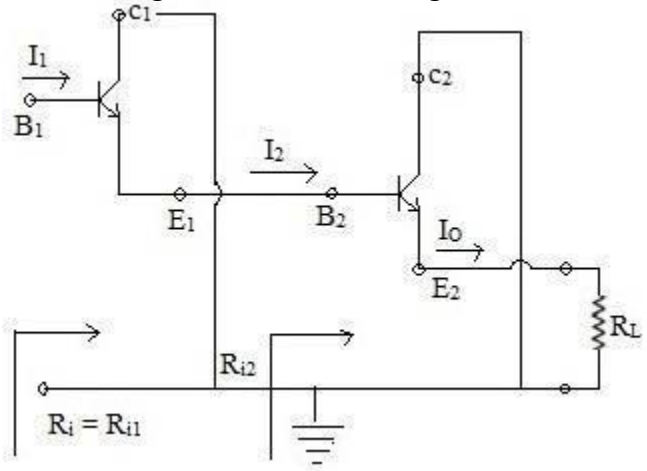
h-parameter equivalent circuit



Darlington pair



Darlington pair 1- Two emitter follower stages in cascade with infinite emitter resistance in the first stage constitute a Darlington circuit.



Second Stage

Let us assume , $h_{oe} R_L < 0.1$

Also $h_{fe} >> 1$

$$A_{I_2} = \frac{I_o}{I_2} = 1 + h_{fe} \simeq h_{fe} \text{ ----- (1)}$$

$R_{i2} = h_{ie} + (1+h_{fe}) R_L \sim h_{ie} + h_{fe} R_L \; h_{fe} R_L$ ----------(2)

$R_{L1} = R_{i2} = h_{fe} R_L$ ---------- (3)

First Stage

$h_{oe}R_{L1} = h_{oe}h_{fe}R_L < 0.1$. If this inequality is satisfied, then we can use simplified equivalent ckt in the first stage.Using exact solution

$$A_{I_1} = \frac{-h_{fe}}{1 + h_{oe} R_{L1}}$$

$$A_{I_1} = \frac{1 + h_{fe}}{1 + h_{oe} h_{fe} R_L} \text{ ------ (4)}$$

$R_{i1} = h_{ie} + h_{rc} A_{I1} R_{L1}$

$$= h_{ie} + \frac{h_{fe}\, h_{fe} R_L}{1 + h_{oe}\, h_{fe} R_L}$$

$$= h_{ie} + \frac{h_{fe}^{\,2} R_L}{1 + h_{oe}\, h_{fe} R_L}$$

For emitter follower

$R_i = h_{ie} + (1+h_{fe})\, R_L$

$= h_{ie} + h_{fe}\, R_L$

Overall current gain

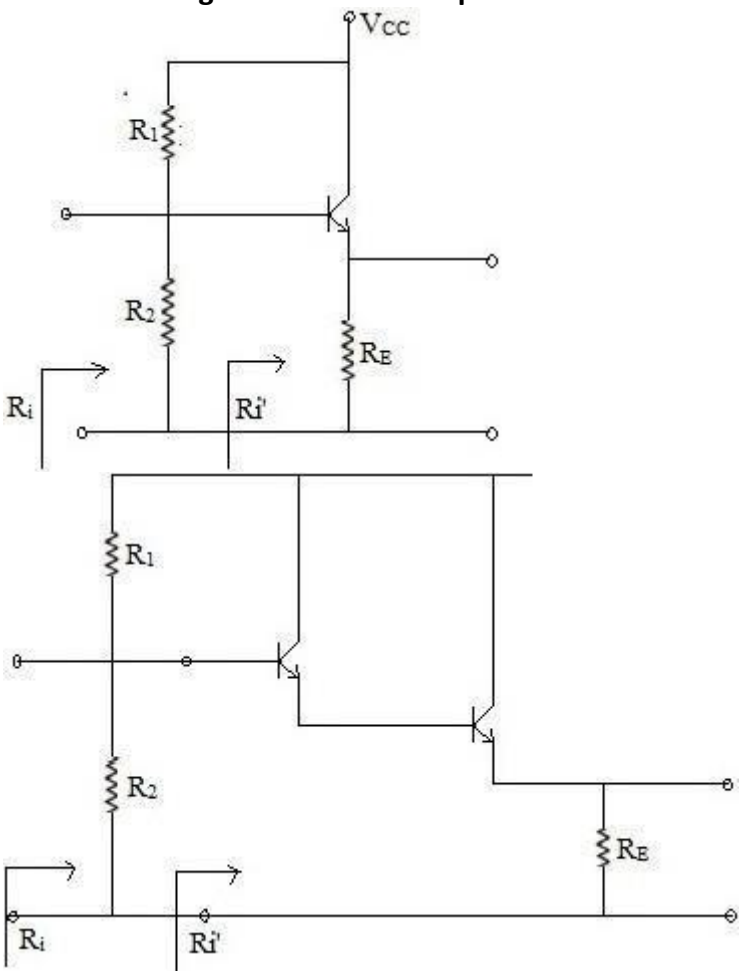
$$A_I = A_1 A_2 = \frac{h_{fe}^{\,2}}{1+h_{oe}\, h_{fe} R_L}$$

Emitter follower, $A_V = \frac{1-h_{ie}}{R_L} - - - - - - - - (1)$

Darlington ckt , $A_V = A_{V1}\, A_{V2}$

$$= \frac{1-h_{ie2}}{R_{i2}} (2 + h_{oe}\, h_{fe} R_L) - - - - - - - (2)$$

Effect of biasing network on the input resistance of emitter follower or Darlington ckt.

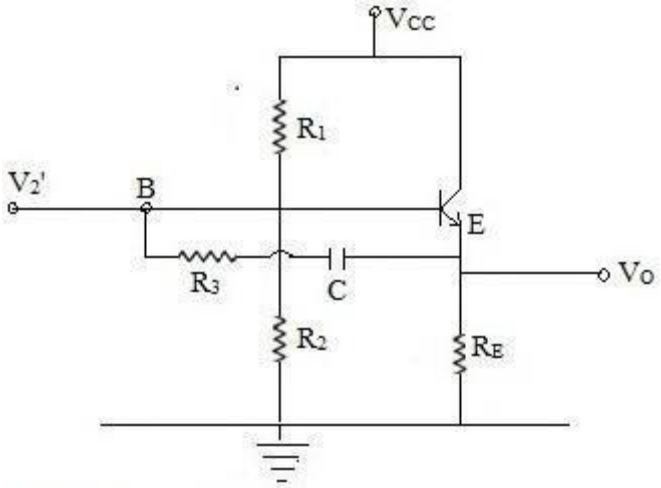


Effective input resistance $R_i = R_1 \,||\, R_2 \,||\, R_i'$ where R_i' is a large input resistance of emitter follower or Darlington ckt.

$R_i = R_B \,||\, R_i'$

$\sim R_B$

Emitter follower with Boot Strap Biasing



The reactance offered by the capacitor is very low for all frequencies.

$$A_V = \frac{V_o}{V_i}$$

$$\therefore \quad V_o = A_V V_i \approx V_i$$

R_3 can be replaced by Miller's theorem

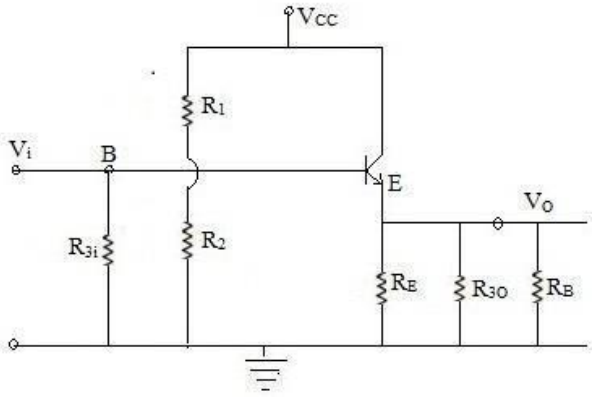
$$R_{3i} = \frac{R_3}{1 - A_V} = \infty$$

$$R_{3O} = \frac{R_3}{1 - 1/A_V} = \frac{R_3 A_V}{A_V - 1}$$

Effective output resistance

$R_L = R_O \,||\, R_{3O} \,||\, R_B$

$\approx R_O$



Coupling Schemes

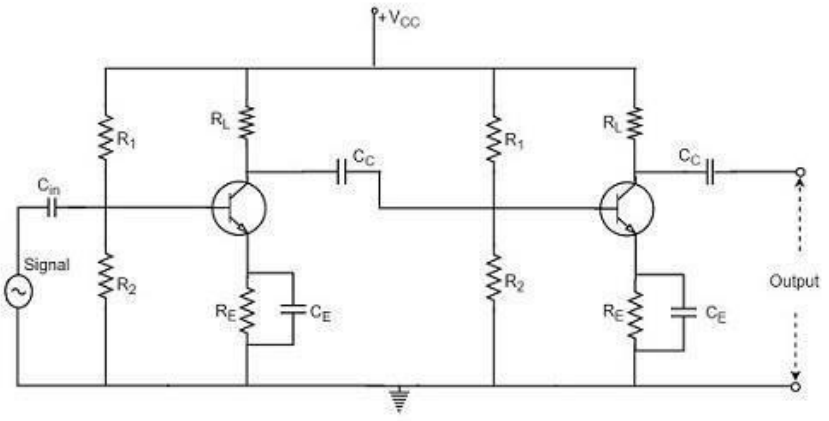
Two-stage RC Coupled Amplifier

The resistance-capacitance coupling is, in short termed as RC coupling. This is the mostly used coupling technique in amplifiers.

Construction ofa Two-stage RC Coupled Amplifier

The constructional details of a two-stage RC coupled transistor amplifier circuit are as follows. The two stage amplifier circuit has two transistors, connected in CE configuration and a common power supply V_{CC} is used. The potential divider network R_1 and $R_2$and the resistor R_e form the biasing and stabilization network. The emitter by-pass capacitor C_e offers a low reactance path to the signal.

The resistor R_L is used as a load impedance. The input capacitor C_{in} present at the initial stage of the amplifier couples AC signal to the base of the transistor. The capacitor C_C is the coupling capacitor that connects two stages and prevents DC interference between the stages and controls the shift of operating point. The figure below shows the circuit diagram of RC coupled amplifier.



Operation of RC Coupled Amplifier

When an AC input signal is applied to the base of first transistor, it gets amplified and appears at the collector load R_L which is then passed through the coupling capacitor C_C to the next stage. This becomes the input of the next stage, whose amplified output again appears across its collector load. Thus the signal is amplified in stage by stage action.

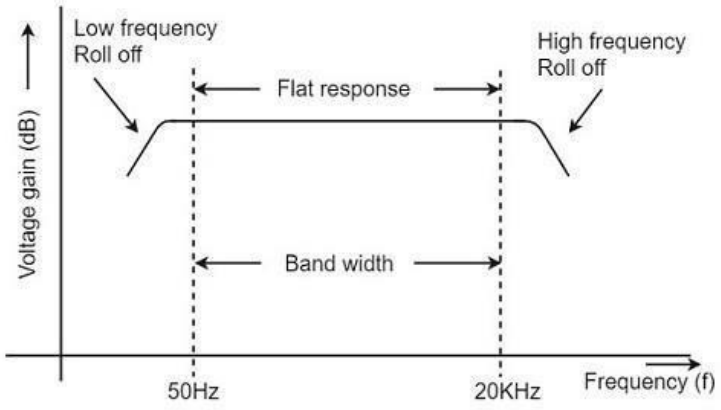
The important point that has to be noted here is that the total gain is less than the product of the gains of individual stages. This is because when a second stage is made to follow the first stage, the **effective load resistance** of the first stage is reduced due to the shunting

effect of the input resistance of the second stage. Hence, in a multistage amplifier, only the gain of the last stage remains unchanged.

As we consider a two stage amplifier here, the output phase is same as input. Because the phase reversal is done two times by the two stage CE configured amplifier circuit.

Frequency Response of RC Coupled Amplifier

Frequency response curve is a graph that indicates the relationship between voltage gain and function of frequency. The frequency response of a RC coupled amplifier is as shown in the following graph.



From the above graph, it is understood that the frequency rolls off or decreases for the frequencies below 50Hz and for the frequencies above 20 KHz. whereas the voltage gain for the range of frequencies between 50Hz and 20 KHz is constant.

We know that,

$$X_C=1/2\pi f_c$$

It means that the capacitive reactance is inversely proportional to the frequency.

At Low frequencies (i.e. below 50 Hz)

The capacitive reactance is inversely proportional to the frequency. At low frequencies, the reactance is quite high. The reactance of input capacitor C_{in} and the coupling capacitor C_C are so high that only small part of the input signal is allowed. The reactance of the emitter by pass capacitor C_E is also very high during low frequencies. Hence it cannot shunt the emitter resistance effectively. With all these factors, the voltage gain rolls off at low frequencies.

At High frequencies (i.e. above 20 KHz): Again considering the same point, we know that the capacitive reactance is low at high frequencies. So, a capacitor behaves as a short

circuit, at high frequencies. As a result of this, the loading effect of the next stage increases, which reduces the voltage gain. Along with this, as the capacitance of emitter diode decreases, it increases the base current of the transistor due to which the current gain (β) reduces. Hence the voltage gain rolls off at high frequencies.

At Mid-frequencies (i.e. 50 Hz to 20 KHz)

The voltage gain of the capacitors is maintained constant in this range of frequencies, as shown in figure. If the frequency increases, the reactance of the capacitor C_C decreases which tends to increase the gain. But this lower capacitance reactive increases the loading effect of the next stage by which there is a reduction in gain.

Due to these two factors, the gain is maintained constant.

AdvantagesofRC CoupledAmplifier

The following are the advantages of RC coupled amplifier.

- The frequency response of RC amplifier provides constant gain over a wide frequency range, hence most suitable for audio applications.
- The circuit is simple and has lower cost because it employs resistors and capacitors which are cheap.
- It becomes more compact with the upgrading technology.

DisadvantagesofRC CoupledAmplifier

The following are the disadvantages of RC coupled amplifier.

- The voltage and power gain are low because of the effective load resistance.
- They become noisy with age.
- Due to poor impedance matching, power transfer will be low.

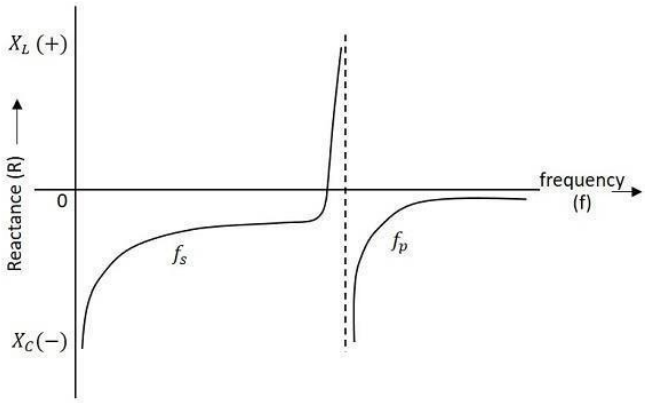
ApplicationsofRC CoupledAmplifier

The following are the applications of RC coupled amplifier.

- They have excellent audio fidelity over a wide range of frequency.
- Widely used as Voltage amplifiers
- Due to poor impedance matching, RC coupling is rarely used in the final stages.

Frequency response

The frequency response of a crystal is as shown below. The graph shows the reactance (X_L or X_C) versus frequency (f). It is evident that the crystal has two closely spaced resonant frequencies.



The first one is the series resonant frequency (f_s), which occurs when reactance of the inductance (L) is equal to the reactance of the capacitance C. In that case, the impedance of the equivalent circuit is equal to the resistance R and the frequency of oscillation is given by the relation,

$$f = \frac{1}{2\pi\sqrt{L.C}}$$

The second one is the parallel resonant frequency (f_p), which occurs when the reactance of R-L-C branch is equal to the reactance of capacitor C_m. At this frequency, the crystal offers a very high impedance to the external circuit and the frequency of oscillation is given by the relation.

$$f_p = \frac{1}{2\pi\sqrt{L.C_T}}$$

Where

$$C_T = \frac{CC_m}{(C + C_m)}$$

The value of C_m is usually very large as compared to C. Therefore, the value of C_T is approximately equal to C and hence the series resonant frequency is approximately equal to the parallel resonant frequency (i.e., $f_s = f_p$).

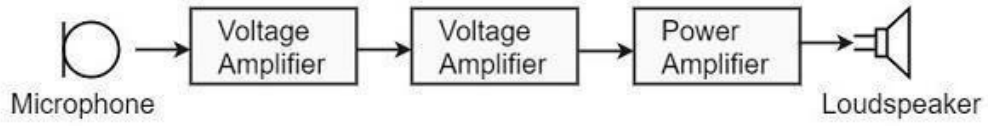
UNIT-III

LARGE SIGNAL AMPLIFIERS

In practice, any amplifier consists of few stages of amplification. If we consider audio amplification, it has several stages of amplification, depending upon our requirement.

Power Amplifier

After the audio signal is converted into electrical signal, it has several voltage amplifications done, after which the power amplification of the amplified signal is done just before the loud speaker stage. This is clearly shown in the below figure.



While the voltage amplifier raises the voltage level of the signal, the power amplifier raises the power level of the signal. Besides raising the power level, it can also be said that a power amplifier is a device which converts DC power to AC power and whose action is controlled by the input signal.

The DC power is distributed according to therelation, DC

power input = AC power output + losses

Power Transistor

For such Power amplification, a normal transistor would not do. A transistor that is manufactured to suit the purpose of power amplification is called as a **Power transistor**.

A Power transistor differs from the other transistors, in the following factors.

- It is larger in size, in order to handle large powers.
- The collector region of the transistor is made large and a heat sink is placed at the collector-base junction in order to minimize heat generated.
- The emitter and base regions of a power transistor are heavily doped.
- Due to the low input resistance, it requires low input power.

Hence there is a lot of difference in voltage amplification and power amplification. So, let us now try to get into the details to understand the differences between a voltage amplifier and a power amplifier.

Difference between Voltage and Power Amplifiers:

Let us try to differentiate between voltage and power amplifier.

Voltage Amplifier

The function of a voltage amplifier is to raise the voltage level of the signal. A voltage

amplifier is designed to achieve maximum voltage amplification.

The voltage gain of an amplifier is given by

$$Av=\beta(Rc/Rin)$$

The characteristics of a voltage amplifier are as follows −

- The base of the transistor should be thin and hence the value of β should be greater than 100.
- The resistance of the input resistor R_{in} should be low when compared to collector load R_C.
- The collector load R_C should be relatively high. To permit high collector load, the voltage amplifiers are always operated at low collector current.
- The voltage amplifiers are used for small signal voltages.

Power Amplifier

The function of a power amplifier is to raise the power level of input signal. It is required to deliver a large amount of power and has to handle large current.

The characteristics of a power amplifier are as follows –

- The base of transistor is made thicken to handle large currents. The value of β being (β > 100) high.
- The size of the transistor is made larger, in order to dissipate more heat, which is produced during transistor operation.
- Transformer coupling is used for impedance matching.
- Collector resistance is made low.

The comparison between voltage and power amplifiers is given below in a tabular form.

S.No	Particular	Voltage Amplifier	Power Amplifier
1	β	High (>100)	Low (5 to 20)
2	R_C	High (4-10 KΩ)	Low (5 to 20 Ω)
3	Coupling	Usually R-C coupling	Invariably transformer coupling
4	Input voltage	Low (a few m V)	High (2-4 V)
5	Collector current	Low (≈ 1 mA)	High (> 100 mA)
6	Power output	Low	High
7	Output impendence	High (≈ 12 K Ω)	Low (200 Ω

The Power amplifiers amplify the power level of the signal. This amplification is done in the last stage in audio applications. The applications related to radio frequencies employ radio power amplifiers. But the **operating point** of a transistor plays a very important role in determining the efficiency of the amplifier. The **main classification** is done based on this mode of operation.

The classification is done based on their frequencies and also based on their mode of operation.

Classification Based on Frequencies

Power amplifiers are divided into two categories, based on the frequencies they handle. They are as follows.

- **Audio Power Amplifiers** − The audio power amplifiers raise the power level of signals that have audio frequency range (20 Hz to 20 KHz). They are also known as **Small signal power amplifiers**.
- **Radio Power Amplifiers** − Radio Power Amplifiers or tuned power amplifiers raise the power level of signals that have radio frequency range (3 KHz to 300 GHz). They are also known as **large signal power amplifiers**.

Classification Based on Mode of Operation

On the basis of the mode of operation, i.e., the portion of the input cycle during which collector current flows, the power amplifiers may be classified as follows.

- **Class A Power amplifier** − When the collector current flows at all times during the full cycle of signal, the power amplifier is known as **class A power amplifier**.
- **Class B Power amplifier** − When the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as **class B power amplifier**.
- **Class C Power amplifier** − When the collector current flows for less than half cycle of the input signal, the power amplifier is known as **class C power amplifier**.

There forms another amplifier called Class AB amplifier, if we combine the class A and class B amplifiers so as to utilize the advantages of both. Before going into the details of these amplifiers, let us have a look at the important terms that have to be considered to determine the efficiency of an amplifier.

Terms Considering Performance

The primary objective of a power amplifier is to obtain maximum output power. In order to

achieve this, the important factors to be considered are collector efficiency, power dissipation capability and distortion. Let us go through them in detail.

Collector Efficiency

This explains how well an amplifier converts DC power to AC power. When the DC supply is given by the battery but no AC signal input is given, the collector output at such a condition is observed as **collector efficiency**.

The collector efficiency is defined as

η=average a.c poweroutput / average d.c powerinputtotransisto

The main aim of a power amplifier is to obtain maximum collector efficiency. Hence the higher the value of collector efficiency, the efficient the amplifier will be.

Power Dissipation Capacity

Every transistor gets heated up during its operation. As a power transistor handles large currents, it gets more heated up. This heat increases the temperature of the transistor, which alters the operating point of the transistor. So, in order to maintain the operating point stability, the temperature of the transistor has to be kept in permissible limits. For this, the heat produced has to be dissipated. Such a capacity is called as Power dissipation capability.

Power dissipation capability can be defined as the ability of a power transistor to dissipate the heat developed in it. Metal cases called heat sinks are used in order to dissipate the heat produced in power transistors.

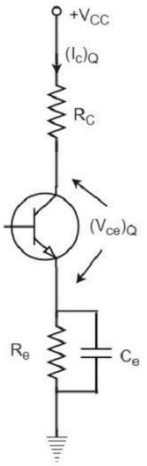
Distortion

A transistor is a non-linear device. When compared with the input, there occur few variations in the output. In voltage amplifiers, this problem is not pre-dominant as small currents are used. But in power amplifiers, as large currents are in use, the problem of distortion certainly arises.

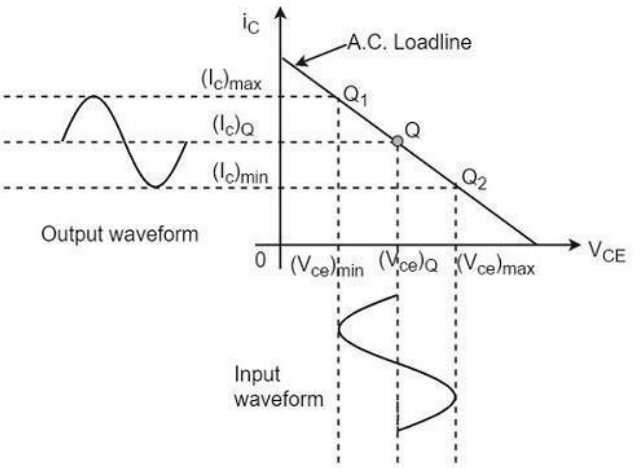
Distortion is defined as the change of output wave shape from the input wave shape of the amplifier. An amplifier that has lesser distortion produces a better output and hence considered efficient.

We have already come across the details of transistor biasing, which is very important for the operation of a transistor as an amplifier. Hence to achieve faithful amplification, the biasing of the transistor has to be done such that the amplifier operates over the linear region.

A Class A power amplifier is one in which the output current flows for the entire cycle of the AC input supply. Hence the complete signal present at the input is amplified at the output. The following figure shows the circuit diagram for Class A Power amplifier.



From the above figure, it can be observed that the transformer is present at the collector as a load. The use of transformer permits the impedance matching, resulting in the transference of maximum power to the load e.g. loud speaker.



The operating point of this amplifier is present in the linear region. It is so selected that the current flows for the entire ac input cycle. The below figure explains the selection of operating point.

The output characteristics with operating point Q is shown in the figure above. Here $(I_c)_Q$ and $(V_{ce})_Q$ represent no signal collector current and voltage between collector and emitter respectively. When signal is applied, the Q-point shifts to Q_1 and Q_2. The output current increases to $(I_c)_{max}$ and decreases to $(I_c)_{min}$. Similarly, the collector-emitter voltage increases to $(V_{ce})_{max}$ and decreases to $(V_{ce})_{min}$.

D.C. Power drawn from collector battery V_{cc} is given by

$$Pin=voltage\times current=V_{CC}(I_C)_Q$$

This power is used in the following two parts −

- Power dissipated in the collector load as heat is given by

$$P_{RC}=(current)^2\times resistance=(IC)^2{}_QR_C$$

- Power given to transistor is given by

$$P_{tr}=P_{in}-P_{RC}=V_{CC}-(I_C)_{2Q}R_C$$

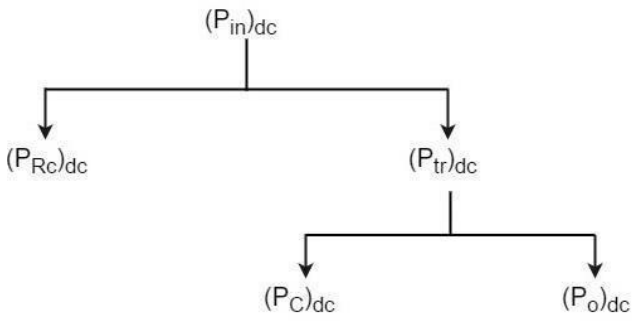
When signal is applied, the power given to transistor is used in the following two parts −

- A.C. Power developed across load resistors RC which constitutes the a.c. power output.

$$(P_O)ac=I^2R_C=V^2/R_C=(V_m/\sqrt{2})/R_C=V2m/2R_C$$

- Where **I** is the R.M.S. value of a.c. output current through load, **V** is the R.M.S. value of a.c. voltage, and $\mathbf{V_m}$ is the maximum value of V.
- The D.C. power dissipated by the transistor (collector region) in the form of heat, i.e., $(P_C)_{dc}$

We have represented the whole power flow in the following diagram.



This class A power amplifier can amplify small signals with least distortion and the output will be an exact replica of the input with increased strength.

Let us now try to draw some expressions to represent efficiencies.

Overall Efficiency

The overall efficiency of the amplifier circuit is given by

$$(\eta)_{overall} = \frac{a.c power\ delivered to the\ load}{total\ power\ delivered by\ d.c\ supply}$$

$$= \frac{(P_O)_{ac}}{(P_{in})_{dc}}$$

Collector Efficiency

The collector efficiency of the transistor is defined as

$$(\eta)_{collector} = \frac{average\ a.c power\ output}{average\ d.c power\ input to transistor}$$

$$= \frac{(P_O)_{ac}}{(P_{tr})_{dc}}$$

Expression for overall efficiency

$$(P_O)_{ac} = V_{rms} \times I_{rms}$$

$$= \frac{1}{\sqrt{2}}\left[\frac{(V_{ce})_{max} - (V_{ce})_{min}}{2}\right] \times \frac{1}{\sqrt{2}}\left[\frac{(I_C)_{max} - (I_C)_{min}}{2}\right]$$

$$= \frac{[(V_{ce})_{max} - (V_{ce})_{min}] \times [(I_C)_{max} - (I_C)_{min}]}{8}$$

Advantages of Class A Amplifiers

The advantages of Class A power amplifier are as follows −

- The current flows for complete input cycle
- It can amplify small signals
- The output is same as input
- No distortion is present

Disadvantages of Class A Amplifiers

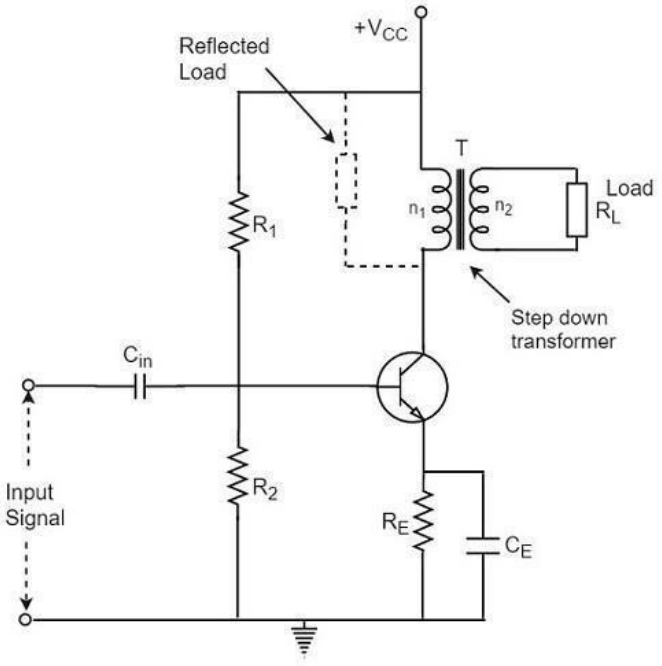
The advantages of Class A power amplifier are as follows −

- Low power output
- Low collector efficiency

The class A power amplifier as discussed in the previous chapter, is the circuit in which the output current flows for the entire cycle of the AC input supply. We also have learnt about the

disadvantages it has such as low output power and efficiency. In order to minimize those effects, the transformer coupled class A power amplifier has been introduced.

The **construction of class A power amplifier** can be understood with the help of below figure. This is similar to the normal amplifier circuit but connected with a transformer in the collector load.

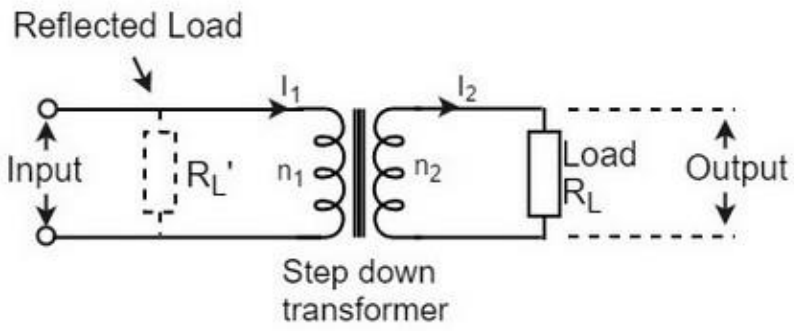


Here R_1 and R_2 provide potential divider arrangement. The resistor Re provides stabilization, C_e is the bypass capacitor and R_e to prevent a.c. voltage. The transformer used here is a step-down transformer.The high impedance primary of the transformer is connected to the high impedance collector circuit. The low impedance secondary is connected to the load (generally loud speaker).

Transformer Action:

The transformer used in the collector circuit is for impedance matching. R_L is the load connected in the secondary of a transformer. R_L' is the reflected load in the primary of the transformer.

The number of turns in the primary are n_1 and the secondary are n_2. Let V_1 and V_2 be the primary and secondary voltages and I_1 and I_2 be the primary and secondary currents respectively. The below figure shows the transformer clearly.



We know that

$$\frac{V_1}{V_2} = \frac{n_1}{n_2} \; and \; \frac{I_1}{I_2} = \frac{n_1}{n_2}$$

Or

$$V_1 = \frac{n_1}{n_2} V_2 \; and \; I_1 = \frac{n_1}{n_2} I_2$$

Hence

$$\frac{V_1}{I_1} = \left(\frac{n_1}{n_2}\right)^2 \frac{V_2}{I_2}$$

But $V_1/I_1 = R_L'$ = effective input resistance

And $V_2/I_2 = R_L$ = effective output resistance

Therefore,

$$R_L' = \left(\frac{n_1}{n_2}\right)^2 R_L = n^2 R_L$$

Where

$$n = \frac{number \; of \; turns \; in \; primary}{number \; of \; turns \; in \; secondary} = \frac{n_1}{n_2}$$

A power amplifier may be matched by taking proper turn ratio in step down transformer.

Circuit Operation

If the peak value of the collector current due to signal is equal to zero signal collector current, then the maximum a.c. power output is obtained. So, in order to achieve complete amplification, the operating point should lie at the center of the load line.

The operating point obviously varies when the signal is applied. The collector voltage varies in opposite phase to the collector current. The variation of collector voltage appears across the primary of the transformer.

Circuit Analysis

The power loss in the primary is assumed to be negligible, as its resistance is very small.

The input power under dc condition will be

$$(P_{in})_{dc} = (P_{tr})_{dc} = V_{CC} \times (I_C)_Q$$

Under maximum capacity of class A amplifier, voltage swings from $(V_{ce})_{max}$ to zero and current from $(I_C)_{max}$ to zero.

Hence

$$V_{rms} = \frac{1}{\sqrt{2}}\left[\frac{(V_{ce})_{max} - (V_{ce})_{min}}{2}\right] = \frac{1}{\sqrt{2}}\left[\frac{(V_{ce})_{max}}{2}\right] = \frac{2V_{CC}}{2\sqrt{2}}$$

$$= \frac{V_{CC}}{\sqrt{2}}$$

$$I_{rms} = \frac{1}{\sqrt{2}}\left[\frac{(I_C)_{max} - (I_C)_{min}}{2}\right] = \frac{1}{\sqrt{2}}\left[\frac{(I_C)_{max}}{2}\right] = \frac{2(I_C)_Q}{2\sqrt{2}}$$

$$= \frac{(I_C)_Q}{\sqrt{2}}$$

Therefore,

$$(P_O)_{ac} = V_{rms} \times I_{rms} = \frac{V_{CC}}{\sqrt{2}} \times \frac{(I_C)_Q}{\sqrt{2}} = \frac{V_{CC} \times (I_C)_Q}{2}$$

Therefore,

$$\text{Collector Efficiency} = \frac{(P_O)_{ac}}{(P_{tr})_{dc}}$$

Or,

$$(\eta)_{collector} = \frac{V_{CC} \times (I_C)_Q}{2 \times V_{CC} \times (I_C)_Q} = \frac{1}{2}$$

$$= \frac{1}{2} \times 100 = 50\%$$

The efficiency of a class A power amplifier is nearly than 30% whereas it has got improved to 50% by using the transformer coupled class A power amplifier.

Advantages

The advantages of transformer coupled class A power amplifier are as follows.

- No loss of signal power in the base or collector resistors.
- Excellent impedance matching is achieved.
- Gain is high.
- DC isolation is provided.

Disadvantages

The disadvantages of transformer coupled class A power amplifier are as follows.

- Low frequency signals are less amplified comparatively.

- Hum noise is introduced by transformers.
- Transformers are bulky and costly.
- Poor frequency response.

Applications

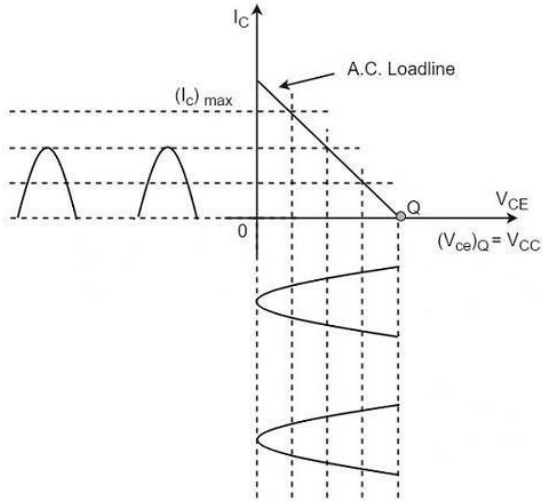
The applications of transformer coupled class A power amplifier are as follows.

- This circuit is where impedance matching is the main criterion.
- These are used as driver amplifiers and sometimes as output amplifiers.
- When the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as **class B power amplifier**.

Class B Operation

The biasing of the transistor in class B operation is in such a way that at zero signal condition, there will be no collector current. The **operating point** is selected to be at collector cut off voltage. So, when the signal is applied, **only the positive half cycle** is amplified at the output.

The figure below shows the input and output waveforms during class B operation.



When the signal is applied, the circuit is forward biased for the positive half cycle of the input and hence the collector current flows. But during the negative half cycle of the input, the circuit is reverse biased and the collector current will be absent. Hence **only the positive half cycle** is amplified at the output.

As the negative half cycle is completely absent, the signal distortion will be high. Also, when the applied signal increases, the power dissipation will be more. But when compared to class A power amplifier, the output efficiency is increased. Well, in order to minimize the disadvantages and achieve low distortion, high efficiency and high output power, the push-pull configuration is used in this class B amplifier.

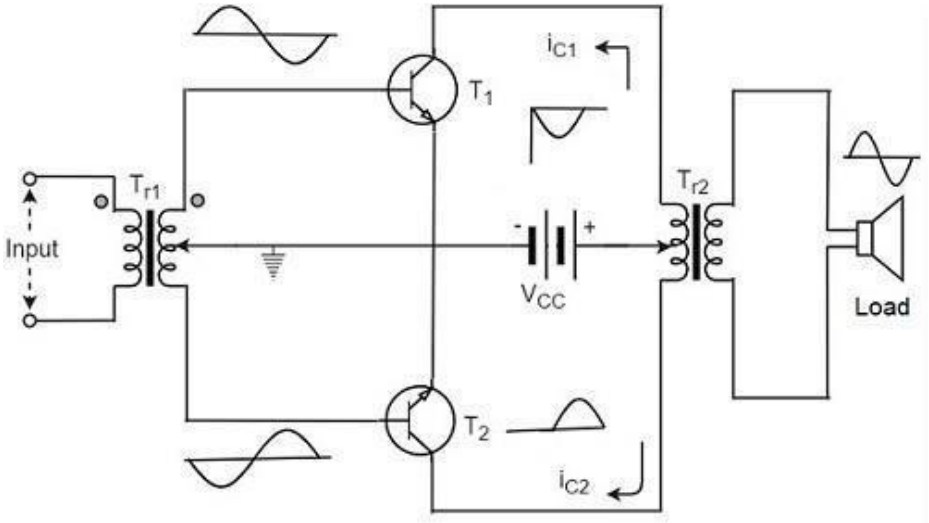
Class B Push-Pull Amplifier

Though the efficiency of class B power amplifier is higher than class A, as only one half cycle of the input is used, the distortion is high. Also, the input power is not completely utilized. In order to compensate these problems, the push-pull configuration is introduced in class B amplifier.

Construction:

The circuit of a push-pull class B power amplifier consists of two identical transistors T_1 and T_2 whose bases are connected to the secondary of the center-tapped input transformer T_{r1}. The emitters are shorted and the collectors are given the V_{CC} supply through the primary of the output transformer T_{r2}.

The circuit arrangement of class B push-pull amplifier, is same as that of class A push-pull amplifier except that the transistors are biased at cut off, instead of using the biasing resistors. The figure below gives the detailing of the construction of a push-pull class B power amplifier.

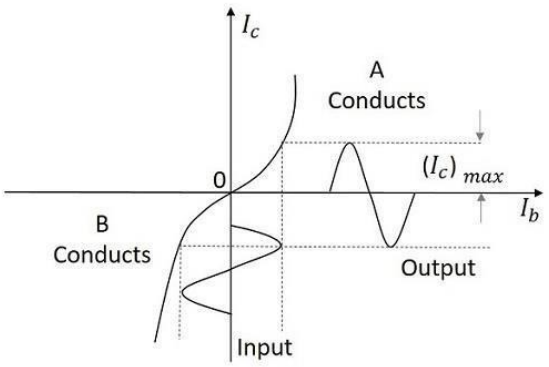


The circuit operation of class B push pull amplifier is detailed below.

Operation

The circuit of class B push-pull amplifier shown in the above figure clears that both the transformers are center-tapped. When no signal is applied at the input, the transistors T_1 and T_2 are in cut off condition and hence no collector currents flow. As no current is drawn from V_{CC}, no power is wasted.

When input signal is given, it is applied to the input transformer T_{r1} which splits the signal into two signals that are 180° out of phase with each other. These two signals are given to the two identical transistors T_1 and T_2. For the positive half cycle, the base of the transistor T_1 becomes positive and collector current flows. At the same time, the transistor T_2 has negative half cycle, which throws the transistor T_2 into cutoff condition and hence no collector current flows. The waveform is produced as shown in the following figure.



For the next half cycle, the transistor T_1 gets into cut off condition and the transistor T_2 gets into conduction, to contribute the output. Hence for both the cycles, each transistor conducts alternately. The output transformer T_{r3} serves to join the two currents producing an almost undistorted output waveform.

Power Efficiency of Class B Push-Pull Amplifier

The current in each transistor is the average value of half sine loop. For half sine loop, I_{dc} is given by $I_{dc} = \frac{(I_C)_{max}}{\pi}$

Therefore,

$$(p_{in})_{dc} = 2 \times \left[\frac{(I_C)_{max}}{\pi} \times V_{CC}\right]$$

Here factor 2 is introduced as there are two transistors in push-pull amplifier.

R.M.S. value of collector current = $(I_C)_{max}/\sqrt{2}$

R.M.S. value of output voltage = $V_{CC}/\sqrt{2}$

Under ideal conditions of maximum power

Therefore,

$$(P_O)_{ac} = \frac{(I_C)_{max}}{\sqrt{2}} \times \frac{V_{CC}}{\sqrt{2}} = \frac{(I_C)_{max} \times V_{CC}}{2}$$

Now overall maximum efficiency

$$\eta_{overall} = \frac{(P_O)_{ac}}{(P_{in})_{dc}}$$

$$= \frac{(I_C)_{max} \times V_{CC}}{2} \times \frac{\pi}{2(I_C)_{max} \times V_{CC}}$$

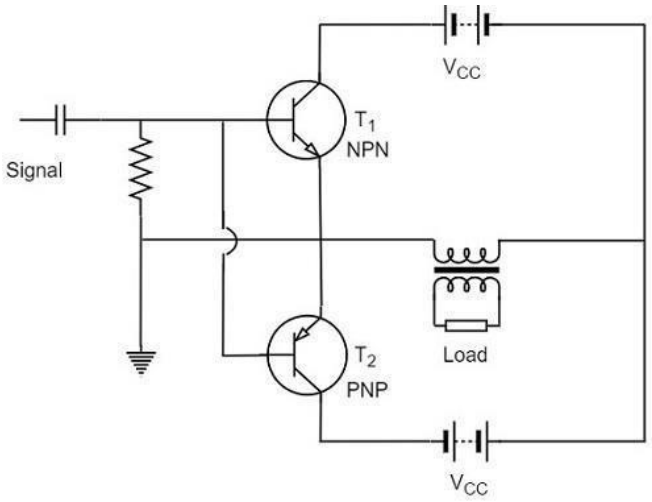
$$= \frac{\pi}{4} = 0.785 = 78.5\%$$

The collector efficiency would be the same.

Hence the class B push-pull amplifier improves the efficiency than the class A push-pull amplifier.

Complementary Symmetry Push-Pull Class B Amplifier

The push pull amplifier which was just discussed improves efficiency but the usage of center-tapped transformers makes the circuit bulky, heavy and costly. To make the circuit simple and to improve the efficiency, the transistors used can be complemented, as shown in the following circuit diagram.



The above circuit employs a NPN transistor and a PNP transistor connected in push pull configuration. When the input signal is applied, during the positive half cycle of the input signal, the NPN transistor conducts and the PNP transistor cuts off. During the negative half cycle, the NPN transistor cuts off and the PNP transistor conducts.

In this way, the NPN transistor amplifies during positive half cycle of the input, while PNP transistor amplifies during negative half cycle of the input. As the transistors are both complement to each other, yet act symmetrically while being connected in push pull configuration of class B, this circuit is termed as **Complementary symmetry push pull class B amplifier**.

Advantages

The advantages of Complementary symmetry push pull class B amplifier are as follows.

- As there is no need of center tapped transformers, the weight and cost are reduced.
- Equal and opposite input signal voltages are not required.

Disadvantages

The disadvantages of Complementary symmetry push pull class B amplifier are as follows.

- It is difficult to get a pair of transistors (NPN and PNP) that have similar characteristics.
- We require both positive and negative supply voltages.

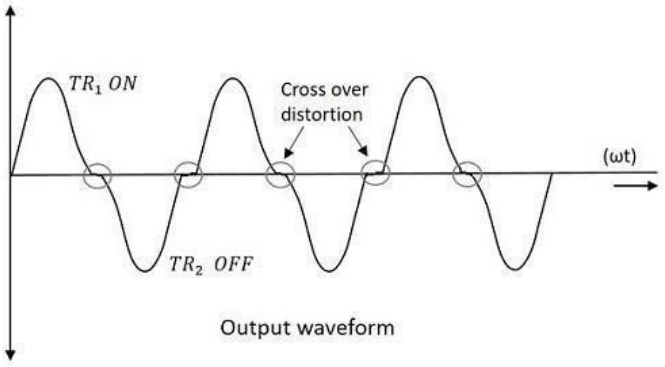
The class A and class B amplifier so far discussed has got few limitations. Let us now try to combine these two to get a new circuit which would have all the advantages of both class A and class B amplifier without their inefficiencies. Before that, let us also go through another important problem, called as **Cross over distortion**, the output of class B encounters with.

Cross-over Distortion:

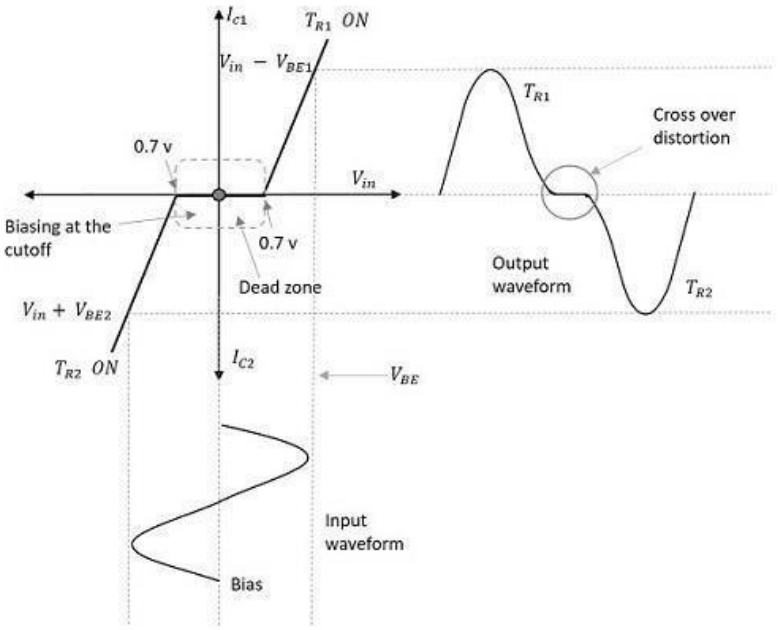
In the push-pull configuration, the two identical transistors get into conduction, one after the other and the output produced will be the combination of both.

When the signal changes or crosses over from one transistor to the other at the zero voltage point, it produces an amount of distortion to the output wave shape. For a transistor in order to conduct, the base emitter junction should cross 0.7v, the cut off voltage. The time taken for a transistor to get ON from OFF or to get OFF from ON state is called the **transition period**.

At the zero voltage point, the transition period of switching over the transistors from one to the other, has its effect which leads to the instances where both the transistors are OFF at a time. Such instances can be called as **Flat spot** or **Dead band** on the output wave shape.



The above figure clearly shows the cross over distortion which is prominent in the output waveform. This is the main disadvantage. This cross over distortion effect also reduces the overall peak to peak value of the output waveform which in turn reduces the maximum power output. This can be more clearly understood through the non-linear characteristic of the waveform as shown below.



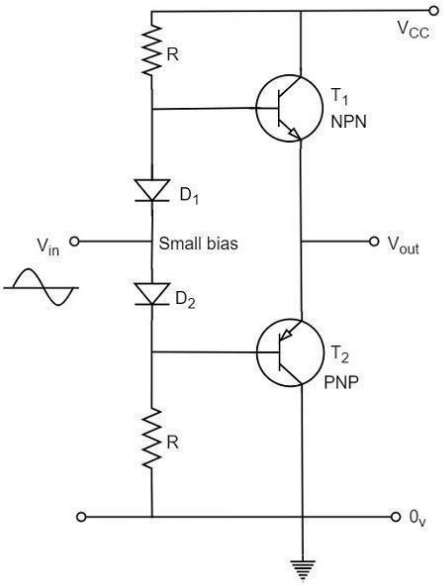
It is understood that this cross-over distortion is less pronounced for large input signals, where as it causes severe disturbance for small input signals. This cross over distortion can be eliminated if the conduction of the amplifier is more than one half cycle, so that both the transistors won't be OFF at the same time.

This idea leads to the invention of class AB amplifier, which is the combination of both class A and class B amplifiers, as discussed below.

Class AB Power Amplifier

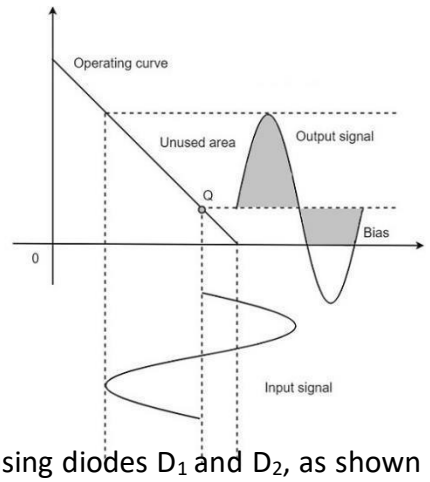
As the name implies, class AB is a combination of class A and class B type of amplifiers. As class A has the problem of low efficiency and class B has distortion problem, this class AB is emerged to eliminate these two problems, by utilizing the advantages of both the classes.

The cross over distortion is the problem that occurs when both the transistors are OFF at the same instant, during the transition period. In order to eliminate this, the condition has to be chosen for more than one half cycle. Hence, the other transistor gets into conduction, before the operating transistor switches to cut off state. This is achieved only by using class AB configuration, as shown in the following circuit diagram.



Therefore, in class AB amplifier design, each of the push-pull transistors is conducting for slightly more than the half cycle of conduction in class B, but much less than the full cycle of conduction of class A.

The conduction angle of class AB amplifier is somewhere between 180° to 360° depending upon the operating point selected. This is understood with the help of below figure.



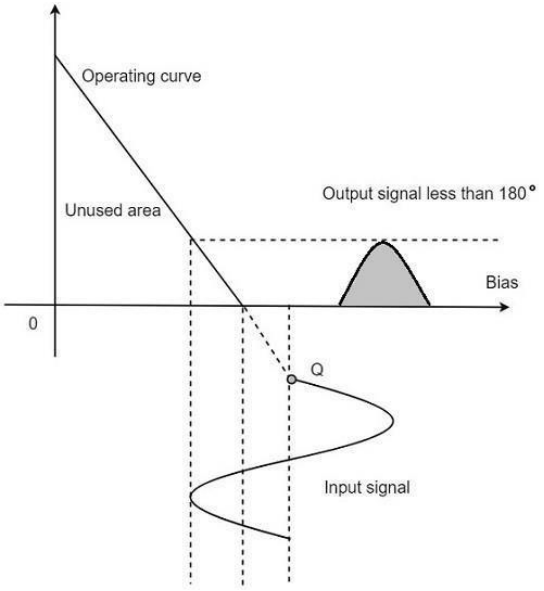
The small bias voltage given using diodes D_1 and D_2, as shown in the above figure, helps the operating point to be above the cutoff point. Hence the output waveform of class AB results as seen in the above figure. The crossover distortion created by class B is overcome by this class AB, as well the inefficiencies of class A and B don't affect the circuit.

So, the class AB is a good compromise between class A and class B in terms of efficiency and linearity having the efficiency reaching about 50% to 60%. The class A, B and AB amplifiers are called as **linear amplifiers** because the output signal amplitude and phase are linearly related to the input signal amplitude and phase.

Class C Power Amplifier

When the collector current flows for less than half cycle of the input signal, the power amplifier is known as **class C power amplifier**. The efficiency of class C amplifier is high while linearity is poor. The conduction angle for class C is less than 180^o. It is generally around 90^o, which means the transistor remains idle for more than half of the input signal. So, the output current will be delivered for less time compared to the application of input signal.

The following figure shows the operating point and output of a class C amplifier.



This kind of biasing gives a much improved efficiency of around 80% to the amplifier, but introduces heavy distortion in the output signal. Using the class C amplifier, the pulses produced at its output can be converted to complete sine wave of a particular frequency by using LC circuits in its collector circuit.

The types of amplifiers that we have discussed so far cannot work effectively at radio frequencies, even though they are good at audio frequencies. Also, the gain of these amplifiers is such that it will not vary according to the frequency of the signal, over a wide range. This allows the amplification of the signal equally well over a range of frequencies and does not permit the selection of particular desired frequency while rejecting the other frequencies.

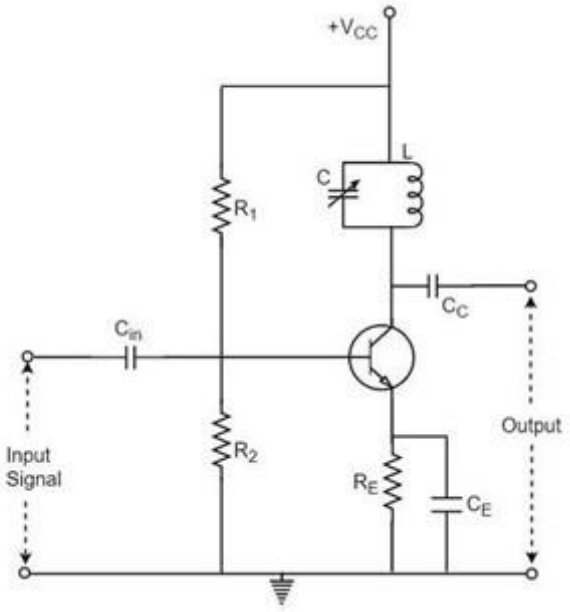
Single Tuned Amplifier

An amplifier circuit with a single tuner section being at the collector of the amplifier circuit is called as Single tuner amplifier circuit.

Construction

A simple transistor amplifier circuit consisting of a parallel tuned circuit in its collector load, makes a single tuned amplifier circuit. The values of capacitance and inductance of the tuned circuit are selected such that its resonant frequency is equal to the frequency to be amplified.

The following circuit diagram shows a single tuned amplifier circuit.



The output can be obtained from the coupling capacitor C_C as shown above or from a secondary winding placed at L.

Operation

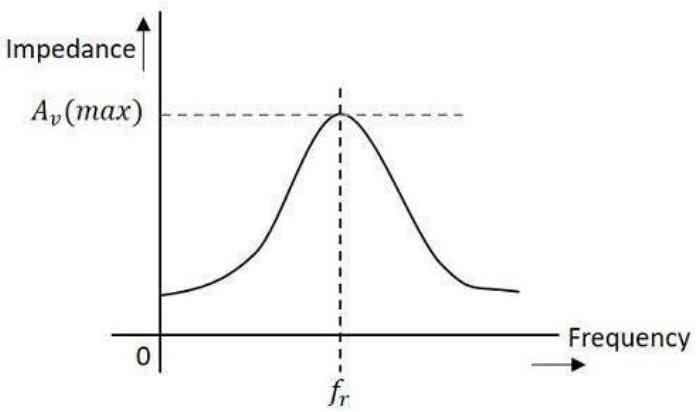
The high frequency signal that has to be amplified is applied at the input of the amplifier. The resonant frequency of the parallel tuned circuit is made equal to the frequency of the signal applied by altering the capacitance value of the capacitor C, in the tuned circuit.At this stage, the tuned circuit offers high impedance to the signal frequency, which helps to offer high output across the tuned circuit. As high impedance is offered only for the tuned frequency, all the other frequencies which get lower impedance are rejected by the tuned circuit. Hence the tuned amplifier selects and amplifies the desired frequency signal.

Frequency Response

The parallel resonance occurs at resonant frequency f_r when the circuit has a high Q. the resonant frequency f_r is given by

$$fr=1/\sqrt{2\pi LC}$$

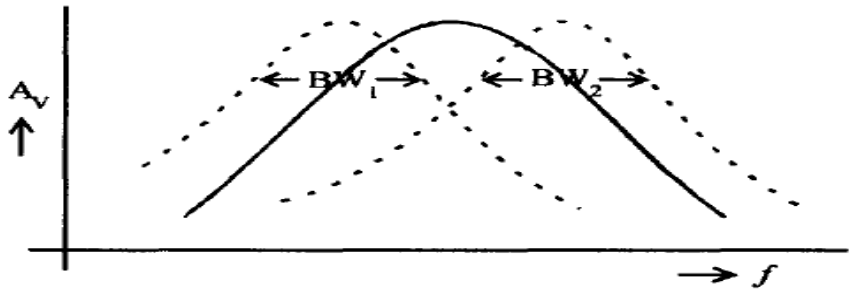
The following graph shows the frequency response of a single tuned amplifier circuit.



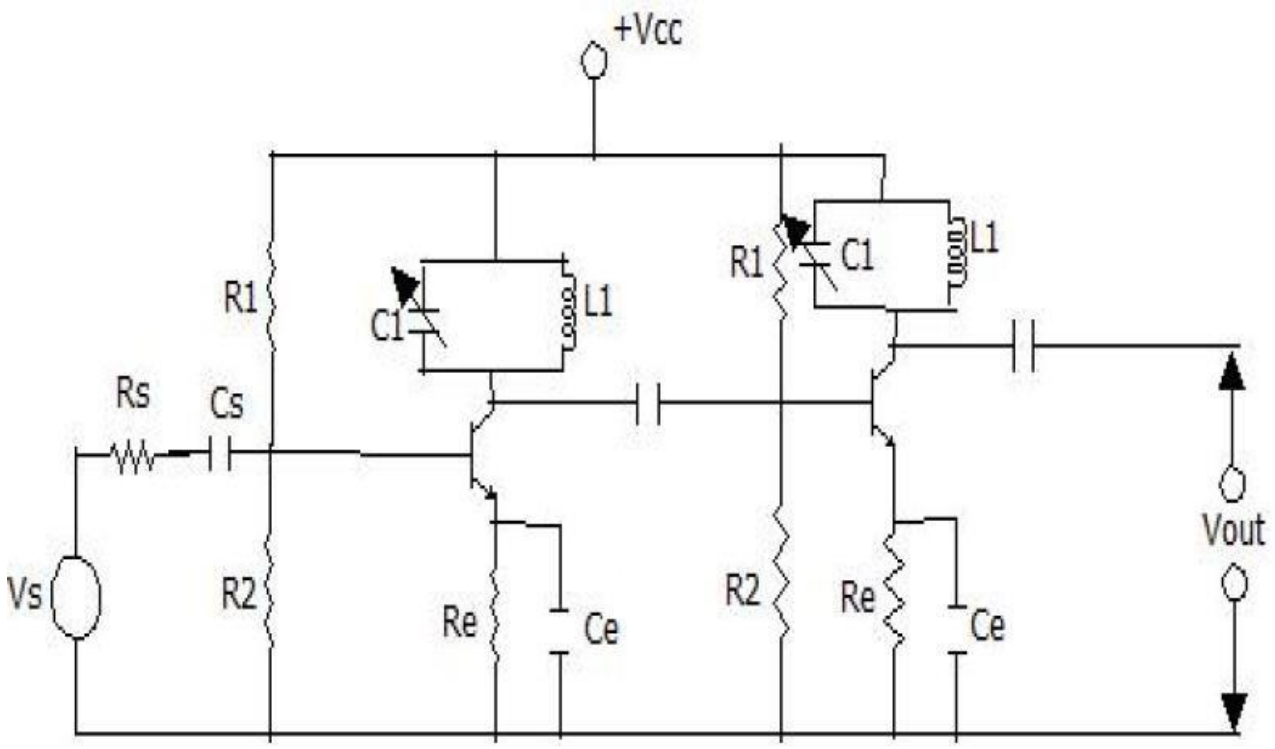
At resonant frequency f_r the impedance of parallel tuned circuit is very high and is purely resistive. The voltage across R_L is therefore maximum, when the circuit is tuned to resonant frequency. Hence the voltage gain is maximum at resonant frequency and drops off above and below it. The higher the Q, the narrower will the curve be.

Stagger Tuning

Tuned amplifiers have large gain, since at resonance, Z is maximum. So Av is maximum. To get this large Av over a wide range of frequencies, stagger tuned amplifiers are employed. This is done by taking two single tuned circuits of a certain Bandwidth, and displacing or staggering their resonance peaks by an amount equal to their Bandwidth. The resultant staggered pair will have a Bandwidth, $\sqrt{2}$ times as great as that of each of individual pairs.



The circuit of stagger tuned amplifier is as shown below:



Stagger Tuned Amplifiers are used to improve the overall frequency response of tuned Amplifiers. Stagger tuned Amplifiers are usually designed so that the overall response exhibits maximal flatness around the centre frequency.

It needs a number of tuned circuit operating in union. The overall frequency response of a Stagger tuned amplifier is obtained by adding the individual response together. Since the resonant Frequencies of different tuned circuits are displaced or staggered, they are referred as Stagger Tuned Amplifier.

The main advantage of stagger tuned amplifier is increased bandwidth. Its Drawback is Reduced Selectivity and critical tuning of many tank circuits. They are used in RF amplifier stage in Radio Receivers.

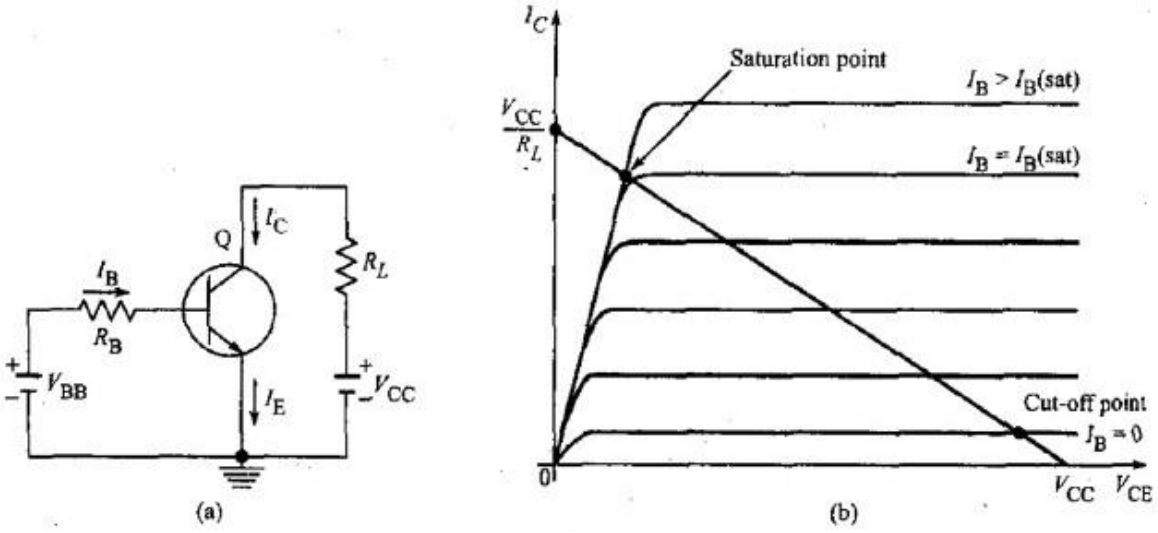
The stagger tuning in this circuit is achieved by resonating the tuned circuits L1 C1, L2 C2 to slightly different Frequencies

UNIT IV
MULTIVIBRATORS

TRANSISTOR AS A SWITCH

A transistor can be used as a switch. It has three regions of operation. When both Emitter-to-base and collector-base junctions are reverse biased, the transistor operates in the cut-off region and it acts as an open switch. When the emitter base junction is forward biased and the Collector base junction is reverse biased, it operates in the active region and acts as auf amplifier. When both the emitter-base and collector-base junctions are forward biased, it Operates in the saturation region and acts as a closed switch. When the transistor is switched! from cut-off to saturation and from saturation to cut-off with negligible active region, the transistor is operated as a switch. When the transistor is in saturation, junction voltages are'i very small but the operating currents are large. When the transistor is in cut-off, the currents* are zero (except small leakage current) but the junction voltages are large.

In Below Figure the transistor Q can be used to connect and disconnect the load *RL* from the source Vcc When Q is saturated it is like a closed switch from collector to emitter and when Q is cutoff it is like an open switch from collector to emitter.



$$I_C = \frac{V_{CC} - V_{CE}}{R_L} \quad \text{and} \quad I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

Referring to the output characteristics shown in Figure (b), the region below the IB = 0 curve is the cut-off region. The intersection of the load line with IB = 0 curve is the cut-off point. At this point, the base current is zero and the collector current is negligible. The emitter diode comes out of forward bias and the normal transistor action is lost, i.e, VCE(cut-off) = *Vcc.* The transistor appears like an open switch.

The intersection of the load line with the IB = IB(sat) curve is called the saturation point. At this point, the base current is IB(sat) and the collector current is maximum. 'At saturation, the collector diode comes out of cut-off and again the normal transistor action is lost, i.e. Ic(sat) = *Vcc / R_L* . IB(sat) represents the minimum base current required to bring the transistor into saturation. For 0 < IB < IB(sat), the transistor operates in the active region. If the base current is greater than IB(sat), the collector current approximately equals Vcc / RL and the transistor appears like a closed switch.

TRANSISTOR SWITCHING TIMES

When the transistor acts as a switch, it is either in cut-off or in saturation. To consider the behaviour of the transistor as it makes transition from one state to the other, consider the circuit shown in below figure (a) driven by the pulse waveform shown in Figure (b). The pulse waveform makes transitions between the voltage levels V2 and V1. At V2 the transistor is at cutoff and at V the transistor is in saturation. The input waveform v; is applied between the base and the emitter through a resistor *RB.*

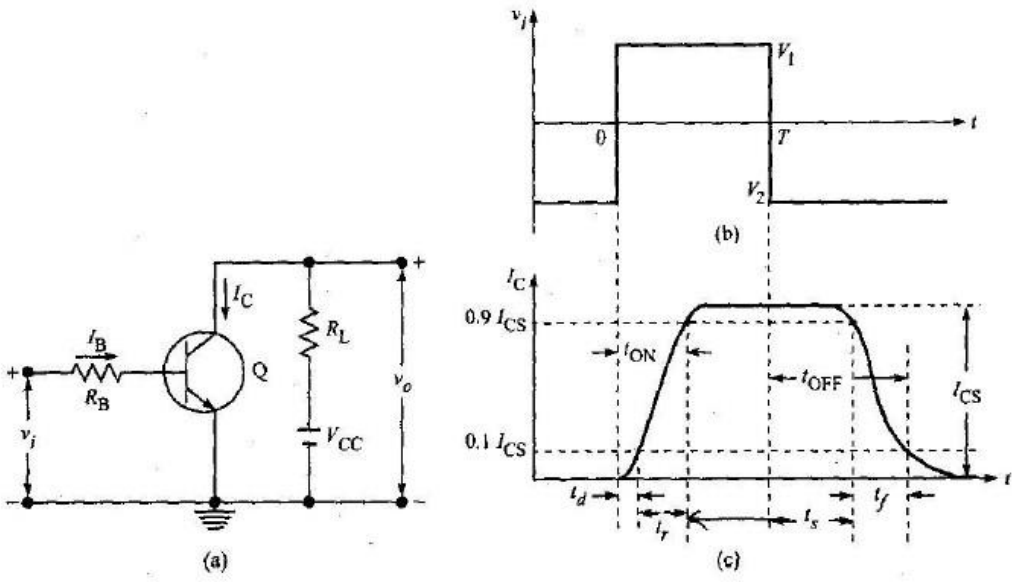


Figure a) Transistor as a Switch b) input waveform c) the response of collector current versus time

The response of the collector current ic to the input waveform, together with its time relationship to the waveform is shown in Figure (c), The collector current does not immediately respond to the input signal. Instead there is a delay, and the time that elapses during this delay, together with the time required for the current to rise to 10% of its maximum (saturation) value (Ics = Vcc / RL)) is called the delay time *td.* The current waveform has a nonzero rise time t r, which

is the rise time required for the current to rise from 10% to 90% of Ics- The total turn-on time TON is the sum of the *delay time* and the rise time, i.e. TON = *td + tr.*

When the input signal returns to its initial state, the collector current again fails to respond immediately. The interval which elapses between the transition of the input waveform and the time when Ic has dropped to 90% of Ics is called the *storage time ts.* The storage interval is followed by the fall time ly, which is the time required for 7C to fall from 90% to 10% of Ics- The turn-off time tOFF is defined as the sum of the storage and fall times, i.e. TOFF = *tr + tf* We shall now consider the physical reasons for the existence of each of these times.

The delay time

There are three factors that contribute to the delay time. First there is a delay which results from the fact that, when the driving signal is applied to the transistor input, a non-zero time is required to charge up the junction capacitance so that the transistor may be brought, from cut-off to the active region. Second, even when the transistor has been brought to the point where minority carriers have begun to cross the emitter junction into the base, a nonzero time is required before these carriers can cross the base region to the collector junction and be recorded as collector current. Finally, a nonzero time is required before the collector current can rise to 10% of its maximum value. Rise time and fall time. The rise time and fall time are due to the fact that, if a base current step is used to saturate the transistor or to return it from saturation into cutoff, the collector current must traverse the active region. The collector current increases or decreases along an exponential curve. Storage time The failure of the transistor to respond to the trailing edge of the driving pulse for the time interval *ts,* results from the fact that a transistor in saturation has a saturation charge of excess minority carriers stored in the base. The transistor cannot respond until the saturation excess charge has been removed.

MULTIVIBRATORS

Multi means many; vibrator means oscillator. A circuit which can oscillate at a number of frequencies is called a multivibrator. Basically there are three types of multivibrators:

1. Bistable multivibrator
2. Monostable multivibrator
3. Astable multivibrator

Each of these multivibrators has two states. As the names indicate, a bistable multivibrator has got two stable states, a monostable multivibrator has got only one stable state (the other state being quasi stable) and the astable multivibrator has got no stable state (both the

states being quasi stable). The stable state of a multivibrator is the state in which the device can stay permanently. Only when a proper external triggering signal is applied, it will change its state. Quasi stable state means temporarily stable state. The device cannot stay permanently in this state. After a predetermined time, the device will automatically come out of the quasi stable state.

Multivibrators find applications in a variety of systems where square waves or timed intervals are required. For example, before the advent of low-cost integrated circuits, chains of multivibrators found use as frequency dividers. A free-running multivibrator with a frequency of one-half to one-tenth of the reference frequency would accurately lock to the reference frequency. This technique was used in early electronic organs, to keep notes of different octaves accurately in tune. Other applications included early television systems, where the various line and frame frequencies were kept synchronized by pulses included in the video signal.

BISTABLE MULTIVIBRATOR

A bistable multivibrator is a multivibrator which can exist indefinitely in either of its two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation. In a bistable multivibrator both the coupling elements are resistors (dc coupling). The bistable multivibrator is also called a multi, Eccles-Jordan circuit (after its inventors), trigger circuit, scale-of-two toggle circuit, flip-flop, and binary. There are two types of bistable multivibrators:

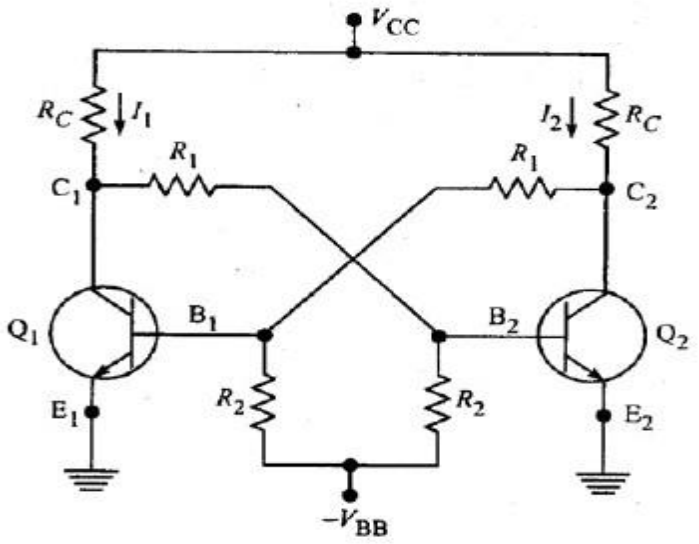
1. Collector coupled bistable multivibrator
2. Emitter coupled bistable multivibrator

There are two types of collector-coupled bistable multivibrators:

1. Fixed-bias bistable multivibrator
2. Self-bias bistable multivibrator

A FIXED-BIAS BISTABLE MULTIVIBRATOR

The Figure below shows the circuit diagram of a fixed-bias bistable multivibrator using transistors (inverters). Note, that the output of each amplifier is direct coupled to the input of the other amplifier.



In one of the stable states, transistor Q[is ON (i.e. in saturation) and Q2 is OFF (i.e. in cut-off), and in the other stable state Qj is OFF and Q2 is ON. Even though the circuit is symmetrical, it is not possible for the circuit to remain in a stable state with both the transistors conducting (i.e. both operating in the active region) simultaneously and carrying equal currents. The reason is that if we assume that both the transistors are biased equally and are carrying equal currents /[and 72 and suppose there is a minute fluctuation in the current *1*\~—let us say it increases by a small amount—then the voltage at the collector of Qi decreases. This will result in a decrease in voltage at the base of Q2. So Q2 conducts less and /2 decreases and hence the potential at the collector of Q2 increases. This results in an increase in the base potential of *Qi.* So, Qi conducts still more and /[is further increased and the potential at the collector of Qt is further reduced, and so on. So, the current *I*\ keeps on increasing and the current /2 keeps on decreasing till Q(goes into saturation and Q2 goes into cut-off. This action takes place because of the regenerative feedback incorporated into the circuit and will occur only if the loop gain is greater than one. *A stable state of a binary is one in which the voltages and currents satisfy the Kirchhoff's laws and are consistent with the device characteristics and in which, in addition, the condition of the loop gain being less than unity is satisfied.*

The condition with respect to loop gain will certainly be satisfied, if either of the two devices is below cut-off or if either device is in saturation. But normally the circuit is designed such that in a stable state one transistor is in saturation and the other one is ir cut-off, because if one transistor is biased to be in cut-off and the other one to be in active region, as the temperature changes or the devices age and the device parameters vary, the quiescent point changes and the quiescent output voltage may also change appreciably Sometimes the drift may

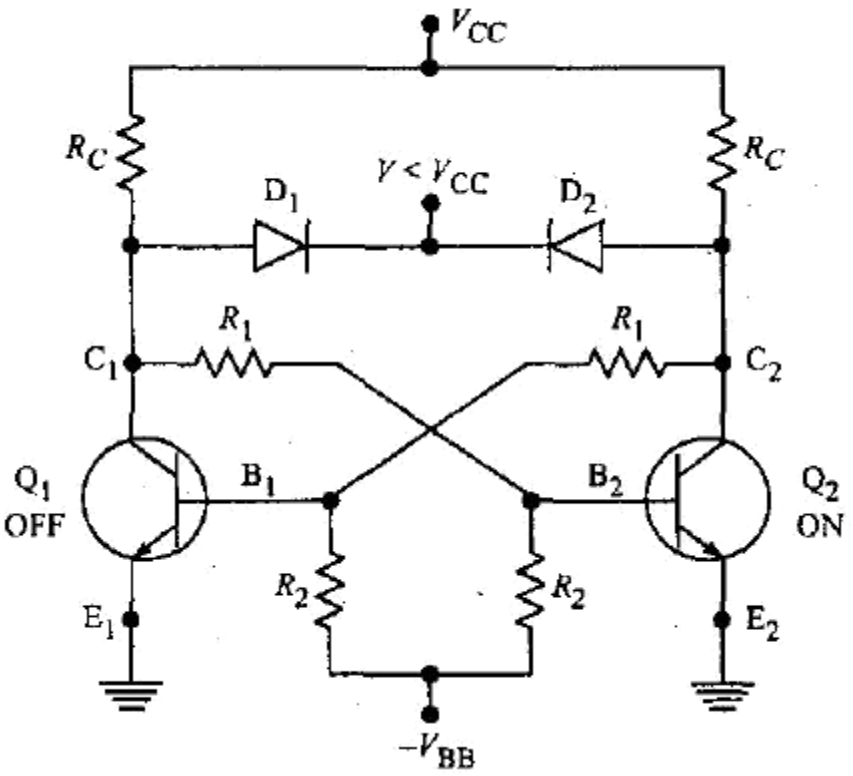
be so much that the device operating in the active region may gc into cut-off, and with both the devices in cut-off the circuit will be useless.

Selection of components in the fixed-bias bistable multivibrator

In the fixed-bias binary shown in Figure 4.1., nearly the full supply voltage Vcc will appear across the transistor that is OFF. Since this supply voltage *Vcc* is to be reasonably smaller than the collector breakdown voltage SVce. *Vcc* restricted to a maximum of a few tens of volts. Under saturation conditions the collector current *Ic* is maximum. Hence *RC* must be chosen so that this value of C (= VCC/^G) does not exceed the maximum permissible limit. The values of *R1, R2* and VBB must be selected such that in one stat>le state the base current is large enough to drive the transistor into saturation whereas in the second stable state the emitter junction must be below cut-off. The signal at a collector called the output swing Vw is the change in collector voltage resulting from a transistor going from one state to the other, i.e. Vw = VCi - IC2- If the loading caused by *RI* can be neglected, then the collector voltage of the OFF transistor is *Vcc.* Since the collector saturation voltage is few tenths of a volt, then the swing Vw = *Vcc,* independently of *RQ*- The component values, the supply voltages and the values of /CBO, *h^,* VBE(sat), and VCE(sat) are sufficient for the analysis of transistor binary circuits.

Loading

The bistable multivibrator may be used to drive other circuits and hence at one or both the collectors there are shunting loads, which are not shown in Figure 4.1. These loads reduce the magnitude of the collector voltage VC1 of the OFF transistor. This will result in reduction of the output voltage swing. A reduced VC[will decrease VB2 and it is possible that Q2 may not be driven into saturation- Hence the flip-flop circuit components must be chosen such that under the heaviest load, which the binary drives, one- transistor remains in saturation while the other is in cut-off. Since the resistor *RI* also loads the OFF transistor, to reduce loading, the value of *R]* should be as large as possible compared to the value of *Rc.* But to ensure a loop gain in excess of unity during the transition between the states, *R^* should be selected such that For some applications, the loading varies with the operation being performed. In such cases, the extent to which a transistor is driven into saturation is variable. A constant output swing V\v = V, arid a constant base saturation current *IB2* can be obtained by clamping the collectors to an auxiliary voltage V < Vcc through the diodes *DI* and D2 as indicated in Figure 4.2. As Qi cuts OFF, its collector voltage rises and when it reaches *V,* the "collector catching diode" D| conducts and clamps the output to *V*.



Standard specifications

In the cut-off region, i.e. for the OFF state

V_{BE} (cut-off) : $\leq$ 0 V for silicon transistor
$\leq$ – 0.1 V for germanium transistor

In the saturation region, i.e. for the ON state

V_{BE} (sat) : 0.7 V for silicon transistor
0.3 V for germanium transistor
V_{CE} (sat) : 0.3 V for silicon transistor
0.1 V for germanium transistor

The above values hold good for n-p-n transistors. For p-n-p transistors the above values with opposite sign are to be taken.

Test for saturation

To test whether a transistor is really in saturation or not evaluate the collector current i_C and the base current i_B independently.

If $i_B > i_B$ (min), where i_B (min) = i_C/h_{FE} (min) the transistor is really in saturation.
If $i_B \leq i_B$ (min), the transistor is not in saturation.

Test for cut-off

To test whether a transistor is really cut-off or not, find its base-to-emitter voltage. If V_{BE} is negative for an n-p-n transistor or positive for a p-n-p transistor, the transistor is really cut-off.

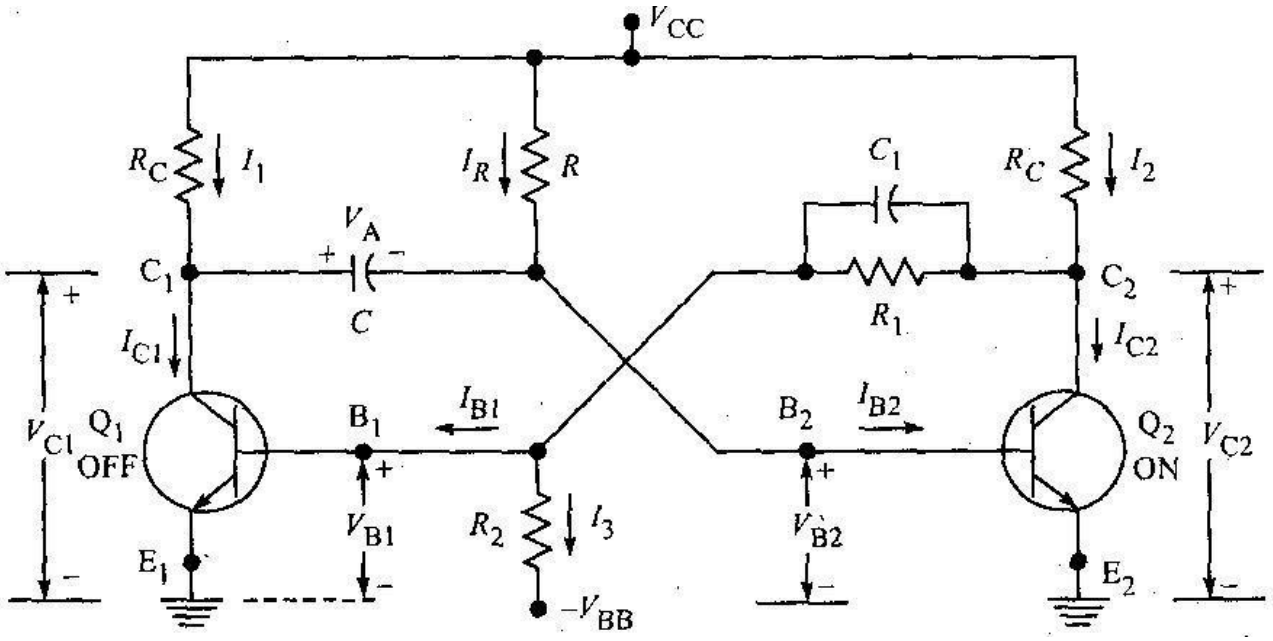
MONOSTABLE MULTIVIBRATOR

Monostable Multivibrators have only **one** stable state (hence their name: "Mono"), and produce a single output pulse when it is triggered externally. Monostable multivibrators only return back to their first original and stable state after a period of time determined by the time constant of the RC coupled circuit.

Monostable multivibrators or "One-Shot Multivibrators" as they are also called, are used to generate a single output pulse of a specified width, either "HIGH" or "LOW" when a suitable external trigger signal or pulse T is applied. This trigger signal initiates a timing cycle which causes the output of the monostable to change its state at the start of the timing cycle and will remain in this second state, which is determined by the time constant of the timing capacitor, CT and the resistor, RT until it resets or returns itself back to its original (stable) state. It will then remain in this original stable state indefinitely until another input pulse or trigger signal is received. Then, **Monostable Multivibrators** have only **ONE** stable state and go through a full cycle in response to a single triggering input pulse.

THE COLLECTOR COUPLED MONOSTABLE MULTIVIBRATOR

The below Figure shows the circuit diagram of a collector-to-base coupled (simply called collectorcoupled) monostable multivibrator using n-p-n transistors. The collector of Q2 is coupled to the base of Qi by a resistor *R}* (dc coupling) and the collector of Qt is coupled to the base of Q2 by a capacitor *C* (ac coupling). Ci is the commutating capacitor introduced to increase the speed of operation. The base of Qi is connected to -VBB through a resistor *R2,* to ensure that Q! is cut off under quiescent conditions. The base of Q2 is connected to VCc through *R* to ensure that Q2 is ON under quiescent conditions. In fact, *R* may be returned to even a small positive voltage but connecting it to *Vcc* is advantageous. The circuit parameters are selected such that under quiescent conditions, the monostable multivibrator finds itself in its permanent stable state with Q2ON (i.e. in saturation) and Q! OFF (i.e. in cut-off)- The multivibrator may be induced to make a transition out of its stable state by the application of a negative trigger at the base of Q2 or at the collector of Q|. Since the triggering signal is applied to only one device and not to both the devices simultaneously, unsymmetrical triggering is employed. When a negative signal is applied at the base of Q2 at $t \sim 0$, due to regenerative action Q2 goes to OFF state and Qi goes to ON state. When Q, is ON, a current /i flows through its *Rc* and hence its collector voltage drops suddenly by *I\RC* This drop will be instantaneously



transmitted through the coupling capacitor C to the base of Q2. So at t = 0+ , the base voltage of Q2 is

$$V_{BE}(\text{sat}) - I_1 R_C$$

The circuit cannot remain in this state for a long time (it stays in this state only for a finite time *T)* because when Qt conducts, the coupling capacitor *C* charges from Vcc through the conducting transistor Qi and hence the potential at the base of Q2 rises exponentially with a time constant

$(R + R_o)C \approx RC,$ where *R0* is the conducting transistor output impedance including the resistance *Rc.* When it passes the cut-in voltage Vy of Q2 (at a time *t = T),* a regenerative action takes place turning Q| OFF and eventually returning the multivibrator to its initial stable state. The transition from the stable state to the quasi-stable state takes place at *t* = 0, and the reverse transition from the quasi-stable state to the stable state takes place at *t = T.* The time *T* for which the circuit is in its quasi-stable state is also referred to as the delay time, and also as the gate width, pulse width, or pulse duration. The delay time may be varied by varying the time constant *t(= RC).*

Expression for the gate width T of a monostable multivibrator neglecting the reverse saturation current /CBO

The below Figure (a) shows the waveform at the base of transistor Q2 of the monostable multivibrator

For *t* < 0, Q2 is ON and so vB2 = VBE(sat). At *t* = 0, a negative signal applied brings Q2 to OFF state and Q[into saturation. A current I flows through *Rc* of Qt and hence vci drops abruptly by I c volts and so vB2 also drops by *I\RC* instantaneously. So at *t* - 0, vB2 = VBE(sat) - *I}RC.* For *t* > 0, the capacitor charges with a time constant *RC,* and hence the base voltage of Q2 rises exponentially towards VCc with the same time constant. At *t* = *T,* when this base voltage rises to the cut-in voltage level Vy of the transistor, Q2 goes to ON state, and Qj to OFF state and the pulse ends. In the interval 0 < *t* < 7", the base voltage of Q2, i.e. vB2 is given by

$$v_{B2} = V_{CC} - (V_{CC} - \{V_{BE}(\text{sat}) - I_1 R_C\})e^{-t/\tau}$$

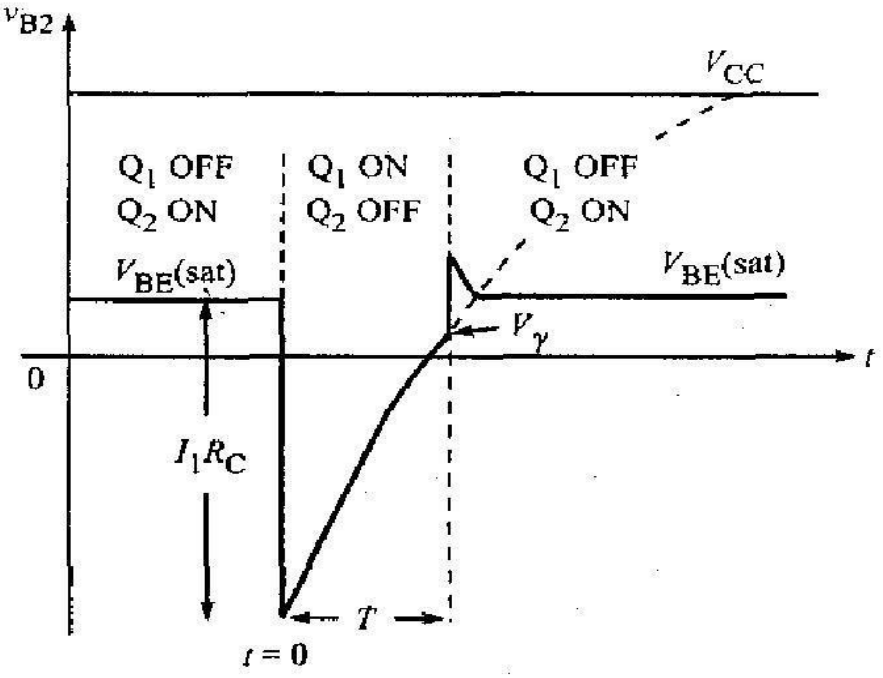


Fig a) Voltage variation at the base of Q2 during the quasi-stable state

But $I_1 R_C = V_{CC} - V_{CE}(\text{sat})$ (because at $t = 0^-$, $v_{C1} = V_{CC}$ and at $t = 0^+$, $v_{C1} = V_{CE}(\text{sat})$)

$$\therefore \quad v_{B2} = V_{CC} - [V_{CC} - \{V_{BE}(\text{sat}) - (V_{CC} - V_{CE}(\text{sat}))\}]e^{-t/\tau}$$

$$= V_{CC} - [2V_{CC} - \{V_{BE}(\text{sat}) + V_{CE}(\text{sat})\}]e^{-t/\tau}$$

At $t = T$, $v_{B2} = V_\gamma$

$$\therefore \quad V_\gamma = V_{CC} - [2V_{CC} - \{V_{CE}(\text{sat}) + V_{BE}(\text{sat})\}]e^{-T/\tau}$$

i.e. $$e^{T/\tau} = \frac{2V_{CC} - [V_{CE}(\text{sat}) + V_{BE}(\text{sat})]}{V_{CC} - V_\gamma}$$

$$\therefore \quad \frac{T}{\tau} = \frac{\text{In}\left[2\left(V_{CC} - \dfrac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}\right)\right]}{V_{CC} - V_\gamma}$$

i.e. $$T = \tau \text{ In } 2 + \tau \text{ In } \frac{V_{CC} - \dfrac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}}{V_{CC} - V_\gamma}$$

Normally for a transistor, at room temperature, the cut-in voltage is the average of the saturation junction

$$V_\gamma = \frac{V_{CE}(sat) + V_{BE}(sat)}{2}$$

voltages for either Ge or Si transistors, i.e.

Neglecting the second term in the expression for *T*

$$T = \tau \ln 2$$

$$T = (R + R_a)C \ln 2 = 0.693(R + R_a)C$$

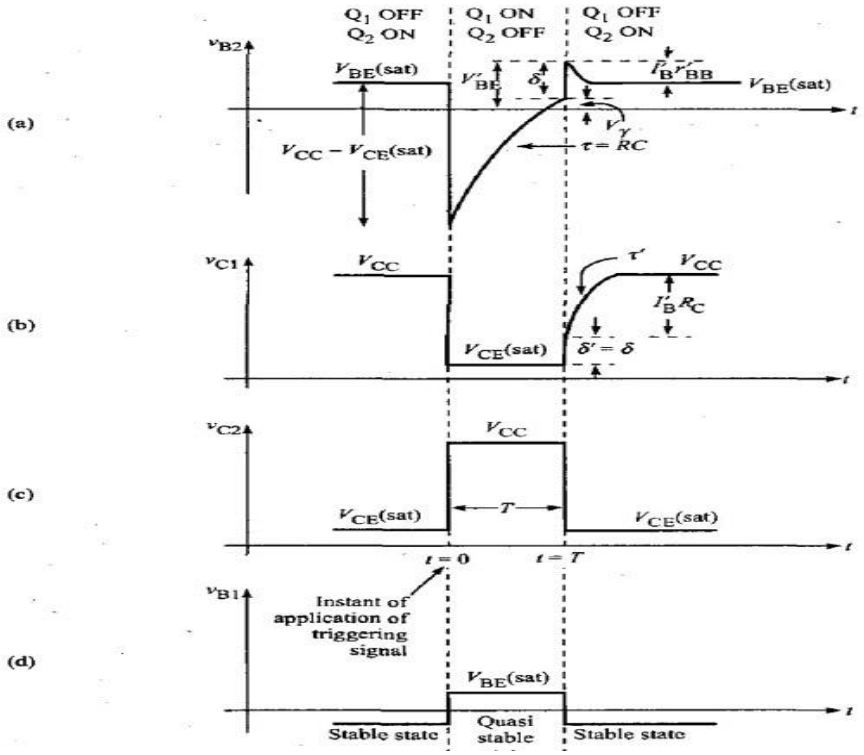
but for a transistor in saturation *Ra « R.*

Gate width, *T* = 0.693RC

The larger the *Vcc* is, compared to the saturation junction voltages, the more accura the result is. The gate width can be made very stable (almost independent of transistor characteristic supply voltages, and resistance values) if Q1 is driven into saturation during the quasi-stab state.

Waveforms of the collector-coupled monostable multivibrator

The waveforms at the collectors and bases of both the transistors Q1 and Q2 are shown below



(a) at the base of Q2, (b) at the collector of Q1, (c) at the collector of Q2, and (d) at the base of Q1

ASTABLE MULTIVIBRATOR

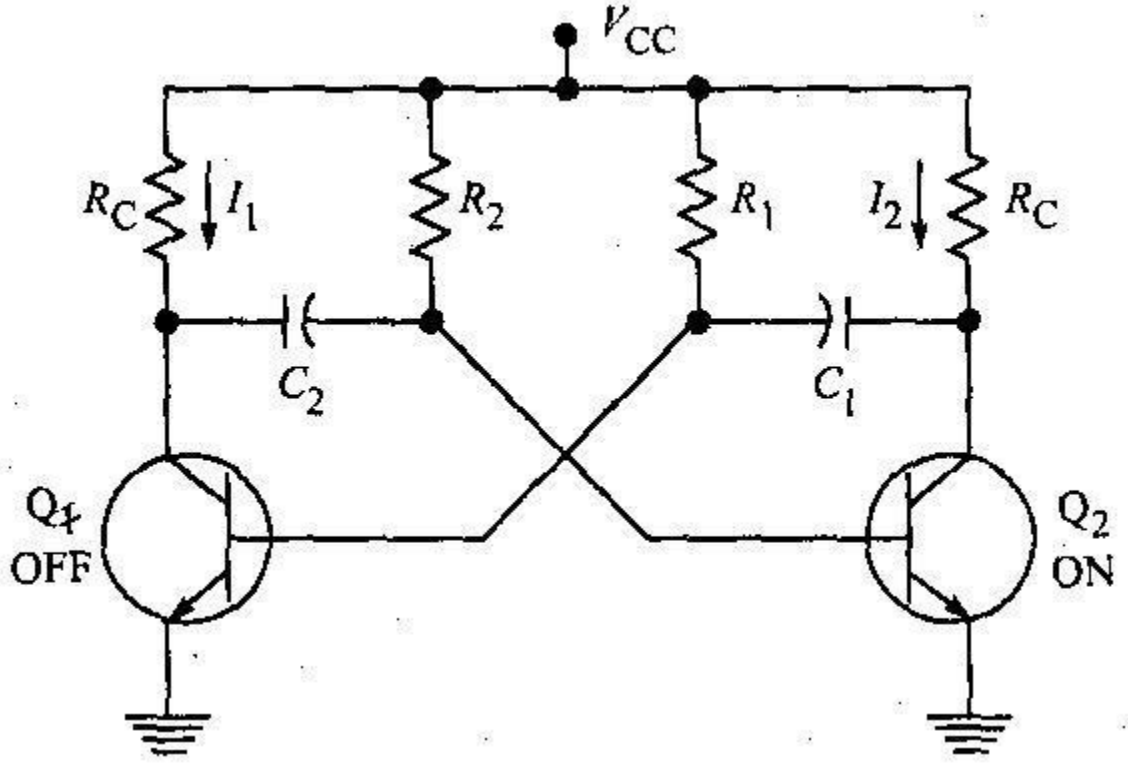
As the name indicates an astable multivibrator is a multivibrator with no permanent stable state. Both of its states are quasi stable only. It cannot remain in any one of its states indefinitely and keeps on oscillating between its two quasi stable states the moment it is connected to the supply. It remains in each of its two quasi stable states for only a short designed interval of time and then goes to the other quasi stable state. No triggering signal is required. Both the coupling elements are capacitors (ac coupling) and hence both the states are quasi stable. It is a free running multivibrator. It generates square waves. It is used as a master oscillator.

There are two types of astable multivibrators:

1. Collector-coupled astable multivibrator
2. Emitter-coupled astable multivibrator

THE COLLECTOR-COUPLED ASTABLE MULTIVIBRATOR

The below Figure shows the circuit diagram of a collector-coupled astable multivibrator using n-p-n transistors. The collectors of both the transistors Qj and Q2 are connected to the bases



of the other transistors through the coupling capacitors Cs and C2. Since both are ac couplings, neither transistor can remain permanently at cut-off. Instead, the circuit has two quasi-stable states, and it makes periodic transitions between these states. Hence it is used as a master oscillator. No triggering signal is required for this multivibrator. The component values are selected such that, the moment it is connected to the supply, due to supply transients one

transistor will go into saturation and the other into cut-off, and also due to capacitive couplings it keeps on-oscillating between its two quasi stable states.

The waveforms at the bases and collectors for the astable multivibrator, are shown in below Figure. Let us say at t = 0, Q2 goes to ON state and Q] to OFF state. So, for t < 0, Q2 was OFF and Q1 was ON

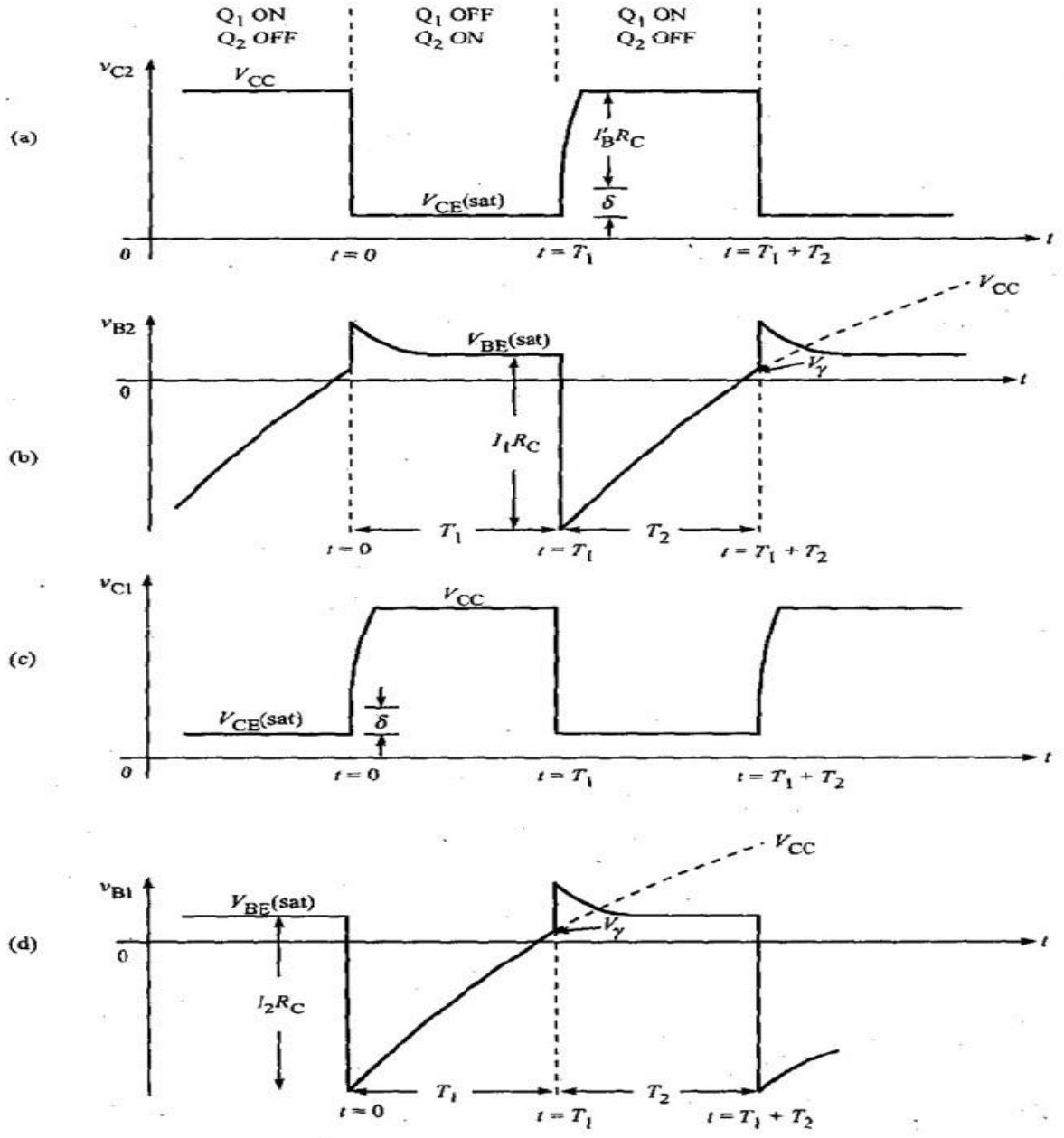


Fig: waveforms at the bases and collectors of a collector-coupled astable multivibrator

Hence for t < 0, vB2 is negative, vC2 = *Vcc,* VB! = VBE(sat) and vcj = VCE(sat). The capacitor C2 charges from Vcc through *R2* and vB2 rises exponentially towards V cc. At t = 0, vB2 reaches the cut-in voltage *Vy* and Q2 conducts. As Q2 conducts, its collector voltage Vc2 drops by /2/?c - ^cc ~ VcE(sa O- This drop in vc2 is transmitted to the base of Qj through the coupling capacitor C2

and hence vB1 also falls by /2/?c- Qi goes to OFF state. So, VB] = VBE(sat) - /2tfc, and its collector voltage vcl rises towards VCc- This rise in vc] is coupled through the coupling capacitor C2 to the base of Q2, causing an overshoot *§* in vB2 and the abrupt rise by the same amount *8* in VCL as shown in Figure 4.51(c). Now since Q2 is ON, *C*\ charges from *Vcc* through *Rlt* and hence VB] rises exponentially. At *t* = 7"], when VB! rises to *VY,* Qi conducts and due to regenerative action Qi goes into saturation and Q2 to cut-off. Now, for *t > T*\, the coupling capacitor C2 charges from Vcc through *R2* and at / = 7", + 7"2, when vB2 rises to the cut-in voltage Vr, Q2 conducts and due to regenerative feedback Q2 goes to ON state and Q| to OFF state. The cycle of events repeats and the circuit keeps on oscillating between its two quasi-stable states. Hence the output is a square wave. It is called a square wave generator or square wave oscillator or relaxation oscillator. It is a free running oscillator.

Expression for the frequency of oscillation of an astable multivibrator

Consider the waveform at the base of Q_1 shown in Figure 4.54(d). At $t = 0$,

$$v_{B1} = V_{BE}(\text{sat}) - I_2R_C$$

But $$I_2R_C = V_{CC} - V_{CE}(\text{sat})$$

$\therefore$ $$\text{At } t = 0,\ v_{B1} = V_{BE}(\text{sat}) - V_{CC} + V_{CE}(\text{sat})$$

For $0 < t < T_1$, v_{B1} rises exponentially towards V_{CC} given by the equation,

$$v_o = v_f - (v_f - v_i)e^{-t/\tau}$$

$\therefore$ $$v_{B1} = V_{CC} - [V_{CC} - (V_{BE}(\text{sat}) - V_{CC} + V_{CE}(\text{sat}))]e^{-t/\tau_1}, \text{ where } \tau_1 = R_1C_1$$

At $t = T_1$, when v_{B1} rises to V_γ, Q_1 conducts

$\therefore$ $$V_\gamma = V_{CC} - [2V_{CC} - (V_{BE}(\text{sat}) + V_{CE}(\text{sat}))]e^{-T_1/R_1C_1}$$

or $$e^{T_1/R_1C_1} = \frac{2\left[V_{CC} - \dfrac{V_{BE}(\text{sat}) + V_{CE}(\text{sat})}{2}\right]}{V_{CC} - V_\gamma}$$

$$T_1 = R_1C_1 \ln \frac{2\left[V_{CC} - \dfrac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}\right]}{V_{CC} - V_\gamma}$$

$$T_1 = R_1C_1 \ln 2 + R_1C_1 \ln \frac{\left[V_{CC} - \dfrac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}\right]}{V_{CC} - V_\gamma}$$

At room temperature for a transistor,

$$V_\gamma \simeq \frac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}$$

$\therefore$ $$T_1 = R_1C_1 \ln 2 = 0.693R_1C_1$$

On similar lines considering the waveform of above Figure , we can show that the time *T2* for which Q2 is OFF and Q1 is ON is given by The period of the waveform, The frequency of oscillation, If *R{ = R2 = R,* and Cs = C2 = C, then TI = *T2* = T.

$$T = 2 \times 0.693RC = 1.386RC \qquad \text{and} \qquad f = \frac{1}{1.386RC}$$

The frequency of oscillation may be varied over the range from cycles to mega cycles by varying *RC.* It is also possible to vary the frequency electrically by connecting *R1* and *R2* to an auxiliary voltage source *V* (the collector supply remains +VCC) and then varying this voltage *V.*

THE EMITTER-COUPLED ASTABLE MULTIVIBRATOR

An emitter-coupled astable multivibrator may be obtained by using three power supplies or a single power supply. The below Figure (a) shows the circuit diagram of a free-running emitter coupled multivibrator using n-p-n transistors. Figure 4.64 shows its waveforms. Three power supplies are indicated for the sake of simplifying the analysis. A more practical circuit using a single supply is indicated in below Figure (b). Let us assume that the circuit operates in such a manner that Q1 switches between cut-off and saturation and Q2 switches between cut-off and its active region.

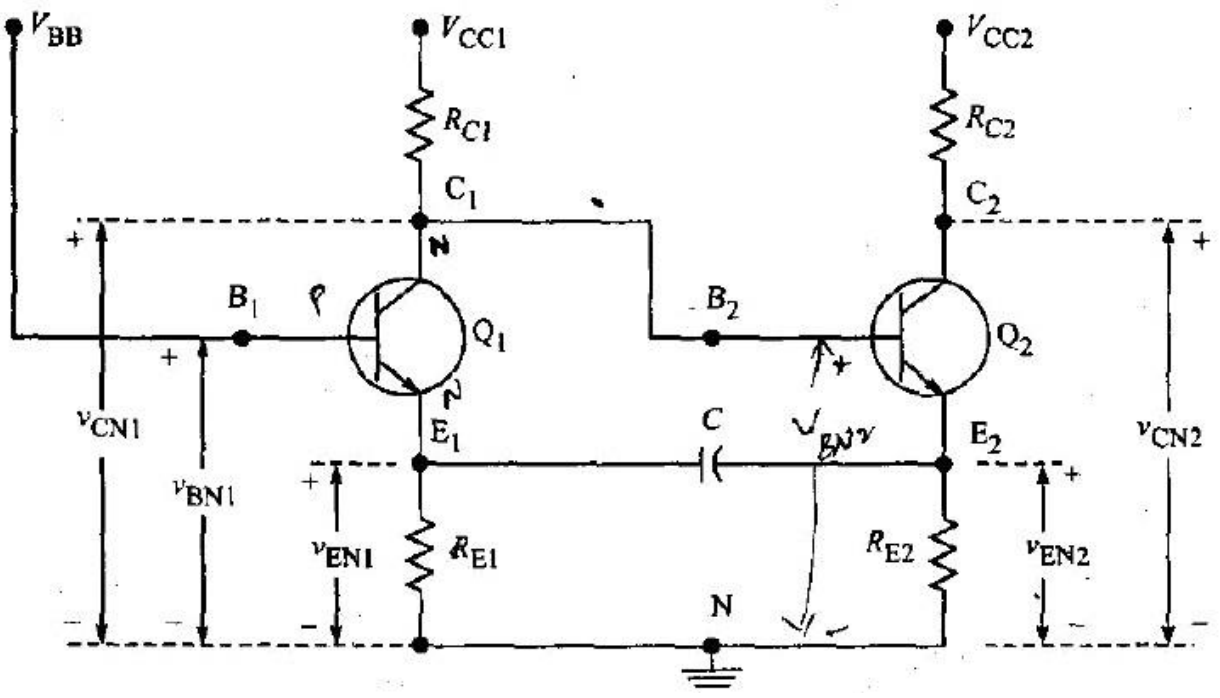


Fig a) Astable Emitter-Coupled Multivibrator

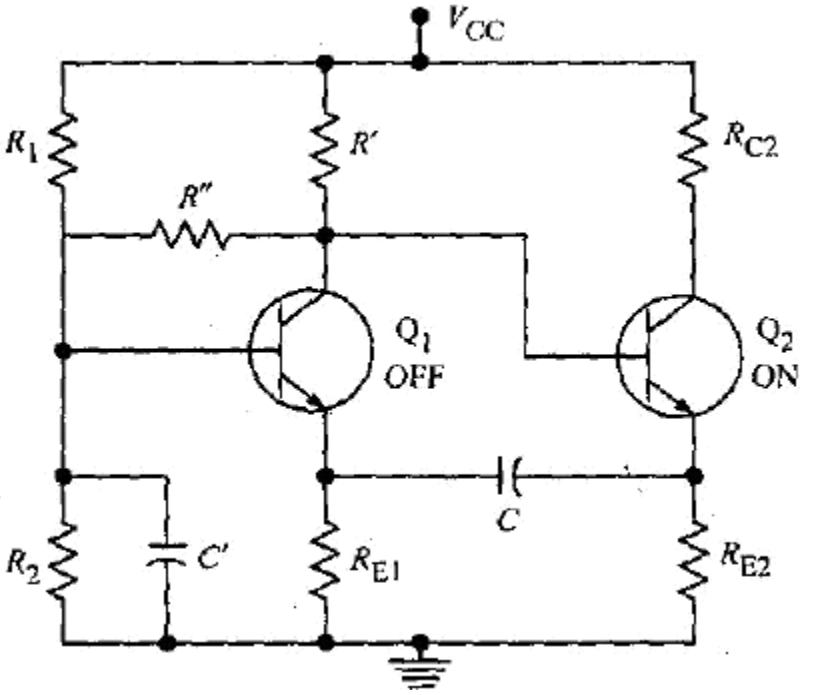


Fig b) Emitter Coupled multivibrator

The waveforms at the base and collector are as shown below:

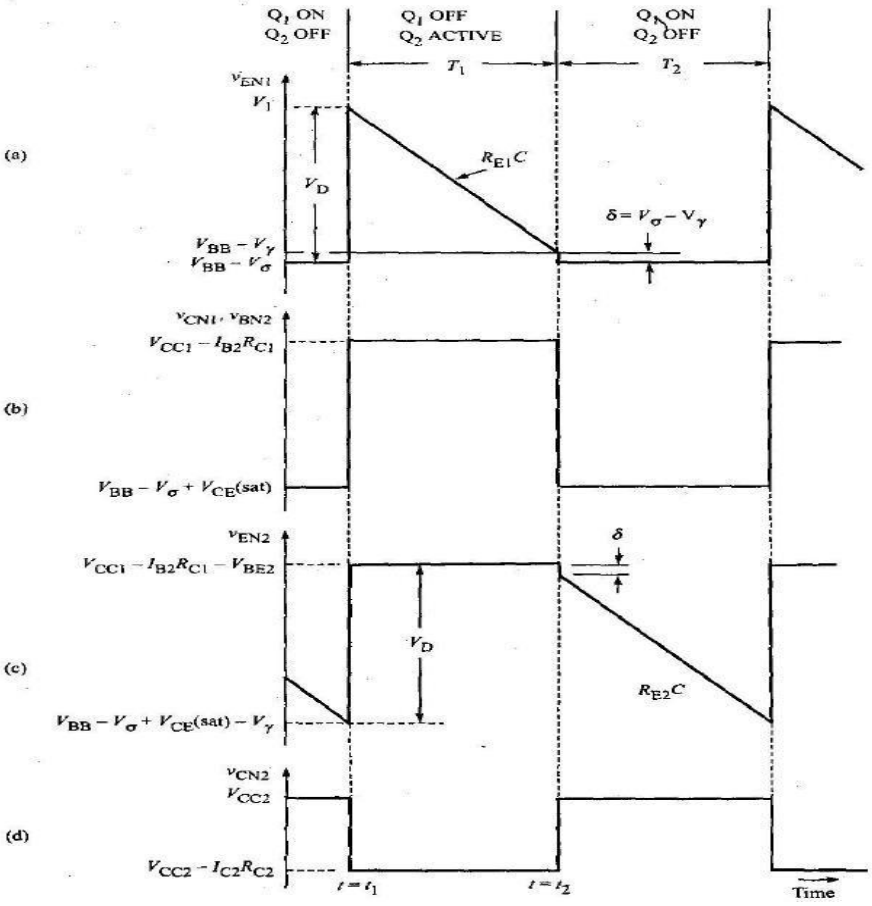


Fig waveforms of the emitter-coupled astable multivibrator

Advantages

1. It is inherently self-starting.
2. The collector of Q2 where the output is taken may be loaded heavily even capacitively.
3. The output is free of recovery transients.
4. Because it has an isolated input at the base of Q1, synchronization is convenient.
5. Frequency adjustment is convenient because only one capacitor is used.

Disadvantages

1. This circuit is more difficult to adjust for proper operating conditions.
2. This circuit cannot be operated with *T1* and T2 widely different.
3. This circuit uses more components than does the collector-coupled circuit.

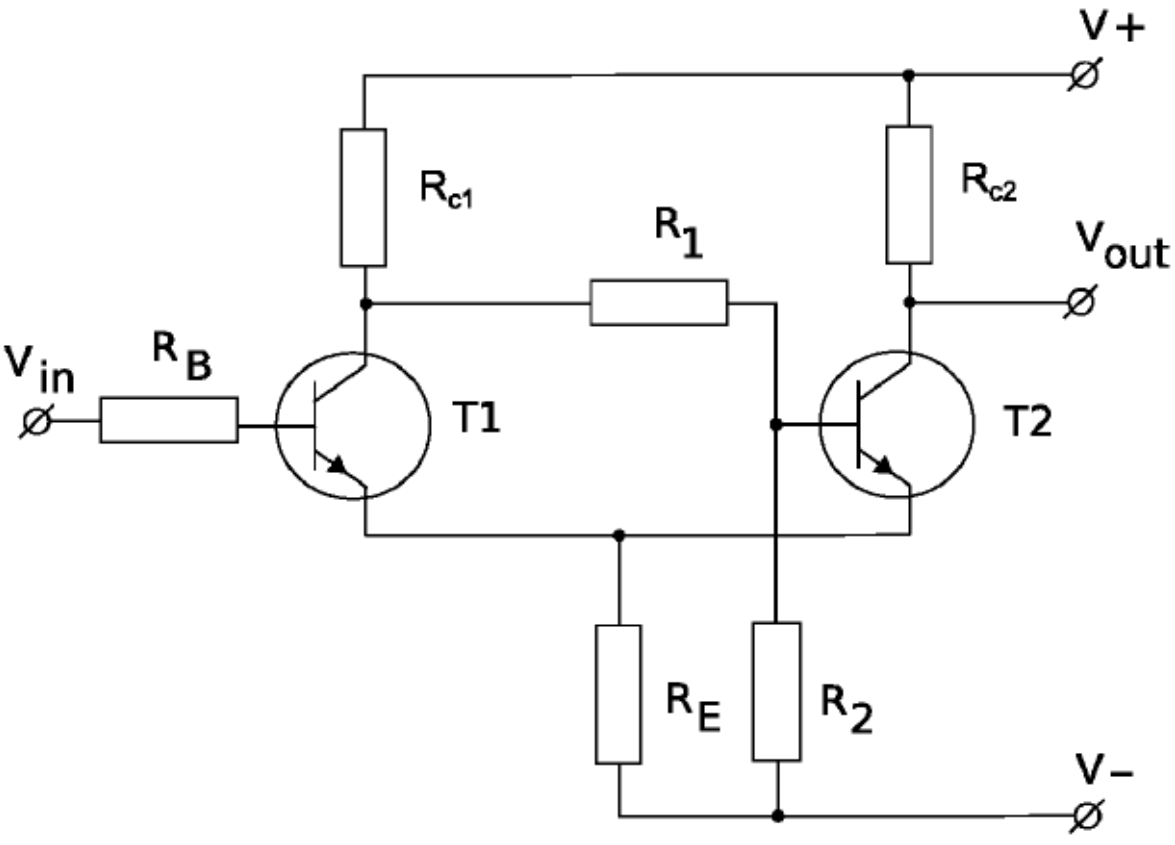
Schmitt trigger

In electronics, **Schmitt trigger** is a circuit with positive feedback and a loop gain >1. The circuit is named "trigger" because the output retains its value until the input changes sufficiently to trigger a change: in the non-inverting configuration, when the input is higher than a certain chosen threshold, the output is high; when the input is below a different (lower) chosen threshold, the output is low; when the input is between the two, the output retains its value. This dual threshold action is called *hysteresis* and implies that the Schmitt trigger possesses memory and can act as a bi-stable circuit (latch). There is a close relation between the two kinds of circuits: a Schmitt trigger can be converted into a latch and a latch can be converted into a Schmitt trigger. Schmitt trigger devices are typically used in open-loop controller configurations for noise immunity and closed loop negative feedback configurations to implement bi-stable regulators, triangle/square wave generators, etc.

The original Schmitt trigger is based on the dynamic threshold idea that is implemented by a voltage divider with a switchable upper leg (the collector resistors Rc1 and Rc2) and a steady lower leg (RE). T1 acts as a comparator with a differential input (T1 base-emitter junction) consisting of an inverting (T1 base) and a non-inverting (T1 emitter) inputs. The input voltage is applied to the inverting input; the output voltage of the voltage divider is applied to the non-inverting input thus determining its threshold. The comparator output drives the second common collector stage T2 (an *emitter follower*) through the voltage follower R1-R2. The emitter-coupled transistors T1 and T2 actually compose an electronic double throw switch that switches over the

upper legs of the voltage divider and changes the threshold in a different (to the input voltage) direction.

This configuration can be considered as a differential amplifier with series positive feedback between its non-inverting input (T2 base) and output (T1 collector) that forces the transition process. There is also a smaller negative feedback introduced by the emitter resistor RE. To make the positive feedback dominate over the negative one and to obtain a hysteresis, the proportion between the two collector resistors is chosen Rc1 > Rc2. Thus less current flows through and less voltage drop is across RE when T1 is switched on than in the case when T2 is switched on. As a result, the circuit has two different thresholds in regard to ground.



Schmitt trigger implemented by two emitter-coupled transistor stages

Operation:

Initial state. For NPN transistors as shown, imagine the input voltage is below the shared emitter voltage (high threshold for concreteness) so that T1 base-emitter junction is backward-biased and T1 does not conduct. T2 base voltage is determined by the mentioned divider so that T2 is conducting and the trigger output is in the low state. The two resistors Rc2 and RE form

another voltage divider that determines the high threshold. Neglecting VBE, the high threshold value is approximately

$$V_{HT} = \frac{R_E}{R_E + R_{c2}} V_+.$$

The output voltage is low but well above the ground. It is approximately equal to the high threshold and may not be low enough to be a logical zero for next digital circuits. This may require additional shifting circuit following the trigger circuit.

Crossing up the high threshold:

When the input voltage (T1 base voltage) rises slightly above the voltage across the emitter resistor RE (the high threshold), T1 begins conducting. Its collector voltage goes down and T2 begins going cut-off, because the voltage divider now provides lower T2 base voltage. The common emitter voltage follows this change and goes down thus making T1 conduct more. The current begins steering from the right leg of the circuit to the left one. Although T1 is more conducting, it passes less current through RE (since Rc1 > Rc2); the emitter voltage continues dropping and the effective T1 base-emitter voltage continuously increases. This avalanche-like process continues until T1 becomes completely turned on (saturated) and T2 turned off. The trigger is transitioned to the high state and the output (T2 collector) voltage is close to V+. Now, the two resistors Rc1 and RE form a voltage divider that determines the low threshold. Its value is approximately

$$V_{LT} = \frac{R_E}{R_E + R_{c1}} V_+.$$

Crossing down the low threshold:

With the trigger now in the high state, if the input voltage lowers enough (below the low threshold), T1 begins cutting-off. Its collector current reduces; as a result, the shared emitter voltage lowers slightly and T1 collector voltage rises significantly. R1-R2 voltage divider conveys this change to T2 base voltage and it begins conducting. The voltage across RE rises, further reducing the T1 base-emitter potential in the same avalanche-like manner, and T1 ceases to conduct. T2 becomes completely turned-on (saturated) and the output voltage becomes low again.

UNIT –V
TIME BASE GENARATORS

TIME BASE GENERATORS

A time-base generator is an electronic circuit which generates an output voltage or current waveform, a portion of which varies linearly with time. Ideally the output waveform should be a ramp. Time-base generators may be voltage time-base generators or current time-base generators. A voltage time-base generator is one that provides an output voltage waveform, a portion of which exhibits a linear variation with respect to time. A current time-base generator is one that provides an output current waveform, a portion of which exhibits a linear variation with respect to time. There are many important applications of time-base generators, such as in CROs, television and radar displays, in precise time measurements, and in time modulation. The most important application of a time-base generator is in CROs. To display the variation with respect to time of an arbitrary waveform on the screen of an oscilloscope it is required to apply to one set of deflecting plates a voltage which varies linearly with time. Since this waveform is used to sweep the electron beam horizontally across the screen it is called the *sweep voltage* and the time-base generators are called the *sweep* circuits.

GENERAL FEATURES OF A TIME-BASE SIGNAL

Figure (a) shows the typical waveform of a time-base voltage. As seen the voltage starting from some initial value increases linearly with time to a maximum value after which it returns again to its initial value. The time during which the output increases is called the *sweep time* and the time taken by the signal to return to its initial value is called the *restoration time,* the *return time,* or *the flyback time.* In most cases the shape of the waveform during restoration time and the restoration time itself are not of much consequence. However, in some cases a restoration time which is very small compared with the sweep time is required. If the restoration time is almost zero and the next linear voltage is initiated the moment the present one is terminated then a saw-tooth waveform shown in (b) is generated. The waveforms of the type shown in Figures (a) and (b) are generally called sweep waveforms even when they are used in applications not involving the deflection of an electron beam. In fact, precisely linear sweep signals are difficult to generate by time-base generators and moreover nominally linear sweep signals may be distorted when transmitted through a coupling

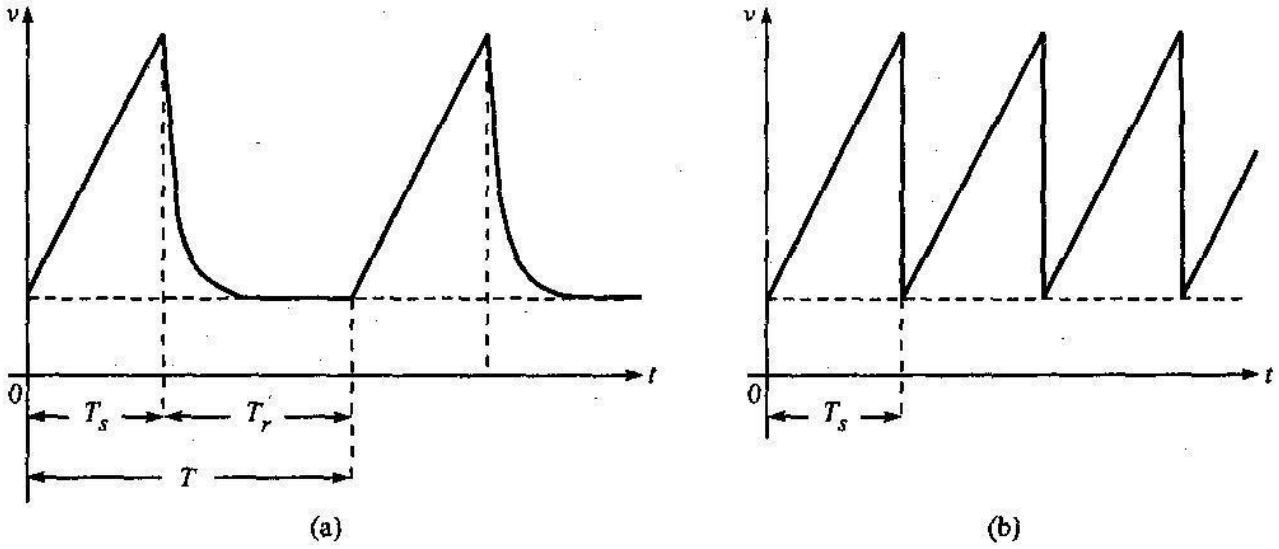


Fig 5.1 (a) General sweep voltage and (b) saw-tooth voltage waveforms.

The deviation from linearity is expressed in three most important ways:
1 . The slope or sweep speed error, *es*
2. The displacement error, *ed*
3. The transmission error, *et*

The slope or sweep-speed error, *es*

An important requirement of a sweep is that it must increase linearly with time, i.e. the rate of change of sweep voltage with time be constant. This deviation from linearity is defined as

$$\text{Slope or sweep-speed error, } e_s = \frac{\text{difference in slope at beginning and end of sweep}}{\text{initial value of slope}}$$

$$= \frac{\left.\frac{dv_0}{dt}\right|_{t=0} - \left.\frac{dv_0}{dt}\right|_{t=T_s}}{\left.\frac{dv_0}{dt}\right|_{t=0}}$$

The displacement error, *ed*

Another important criterion of linearity is the maximum difference between the actual sweep voltage and the linear sweep which passes through the beginning and end points of the actual sweep. The displacement error *ed* is defined as

$$e_d = \frac{\text{maximum difference between the actual sweep voltage and the linear sweep which passes through the beginning and end points of the actual sweep}}{\text{amplitude of the sweep at the end of the sweep time}}$$

$$= \frac{(v_s - v_s')_{\max}}{V_s}$$

As shown in Figure (a), *vs* is the actual sweep and *v's* is the linear sweep.

The transmission error, *et*

When a ramp signal is transmitted through a high-pass circuit, the output falls away from the input as shown in Figure (b). This deviation is expressed as transmission error *et,* defined as the difference between the input and the output divided by the input at the end of the sweep

$$e_t = \frac{V_s' - V_s}{V_s'}$$

where as shown in Figure (b), *V's* is the input and *Vs* is the output at the end of the sweep, i.e. at *t* = TS

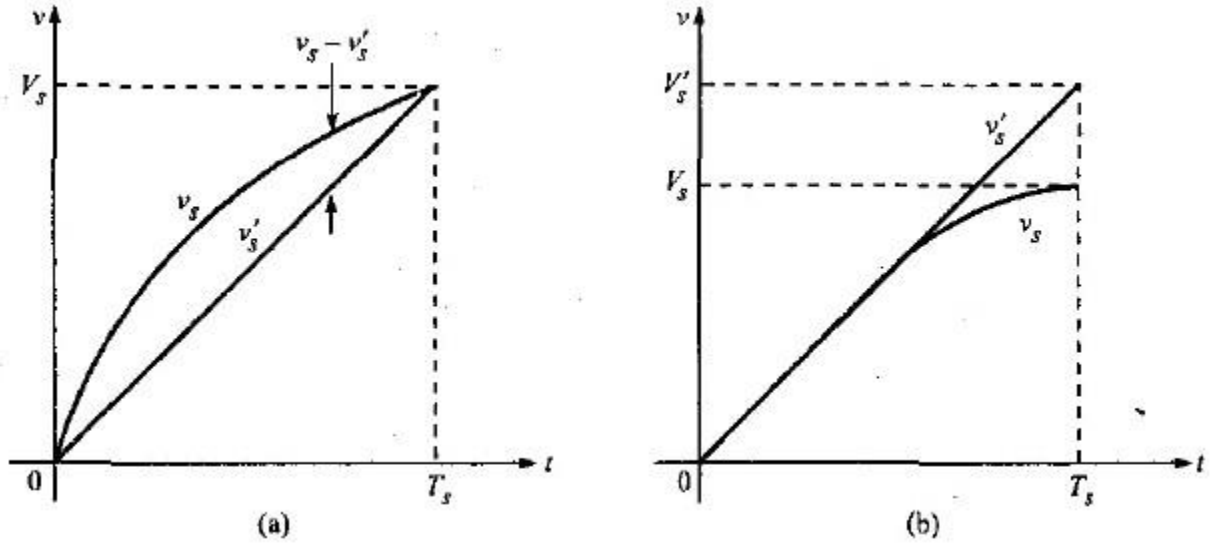


Fig.5.2 (a) Sweep for displacement error and (b) sweep for transmission error

If the deviation from linearity is small so that the sweep voltage may be approximated by the sum of linear and quadratic terms in *t,* then the above three errors are related as :

$$e_d = \frac{e_s}{8} = \frac{e_t}{4}$$

$$e_s = 2e_t = 8e_d$$

which implies that the sweep speed error is the more dominant one and the displacement error is the least severe one.

METHODS OF GENERATING A TIME-BASE WAVEFORM

In time-base circuits, sweep linearity is achieved by one of the following methods.

1. ***Exponential charging.*** In this method a capacitor is charged from a supply voltage through a resistor to a voltage which is small compared with the supply voltage.

2. ***Constant current charging***. In this method a capacitor is charged linearly from a constant current source. Since the charging current is constant the voltage across the capacitor increases linearly.

3. ***The Miller circuit***. In this method an operational integrator is used to convert an input step voltage into a ramp waveform.

4. ***The Phantastron circuit***. In this method a pulse input is converted into a ramp. This is a version of the Miller circuit.

5. ***The bootstrap circuit***. In this method a capacitor is charged linearly by a constant current which is obtained by maintaining a constant voltage across a fixed resistor in series with the capacitor.

6. ***Compensating networks***. In this method a compensating circuit is introduced to improve the linearity of the basic Miller and bootstrap time-base generators.

7. ***An inductor circuit***. In this method an *RLC* series circuit is used. Since an inductor does not allow the current passing through it to change instantaneously, the current through the capacitor more or less remains constant and hence a more linear sweep is obtained.

MILLER AND BOOTSTRAP TIME-BASE GENERATORS—BASIC PRINCIPLES

The linearity of the time-base waveforms may be improved by using circuits involving feedback. Figure 5.3 (a) shows the basic exponential sweep circuit in which S opens to form the sweep. A linear sweep cannot be obtained from this circuit because as the capacitor charges, the charging current decreases and hence the rate at which the capacitor charges, i.e. the slope of the output waveform decreases. A perfectly linear output can be obtained if the initial charging current / = *VIR* is maintained constant. This can be done by introducing an auxiliary variable generator v whose generated voltage v is always equal to and opposite to the voltage across the capacitor as shown in Figure 5.3 (b). Two methods of simulating the fictitious generator are discussed below

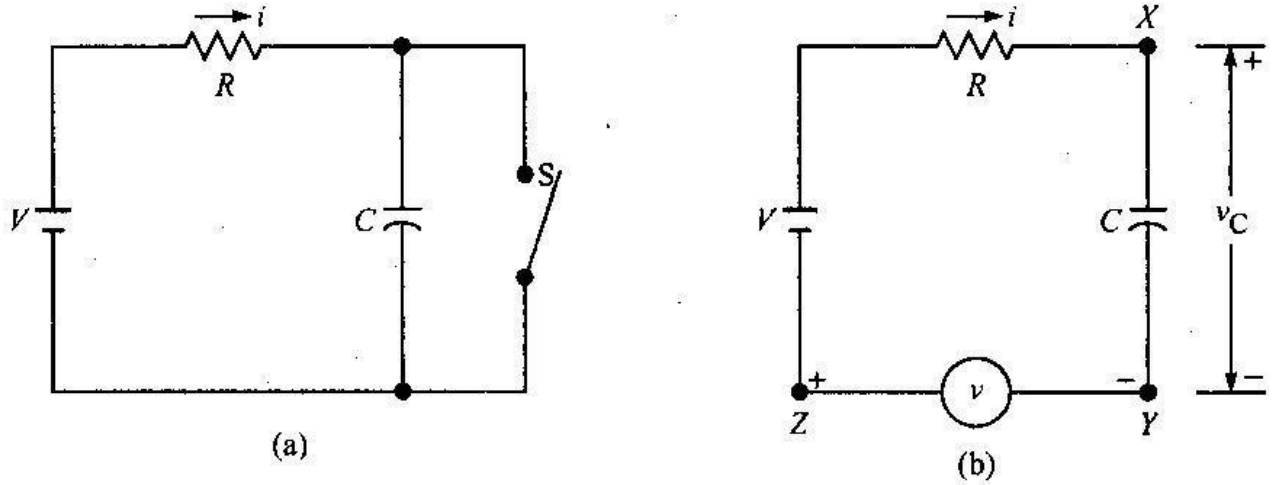


Fig. 5.3 (a) The current decreases exponentially with time and (b) the current remains constant

In the circuit of Figure 5.3 (b) suppose the point Z is grounded as in below Figure 5.4 (a). A linear sweep will appear between the point Y and ground and will increase in the negative direction. Let us now replace the fictitious (imaginary) generator by an amplifier with output terminals YZ and input terminals XZ as shown in below Figure 5.4 (b). Since we have assumed that the generated voltage is always equal and opposite to the voltage across the capacitor,

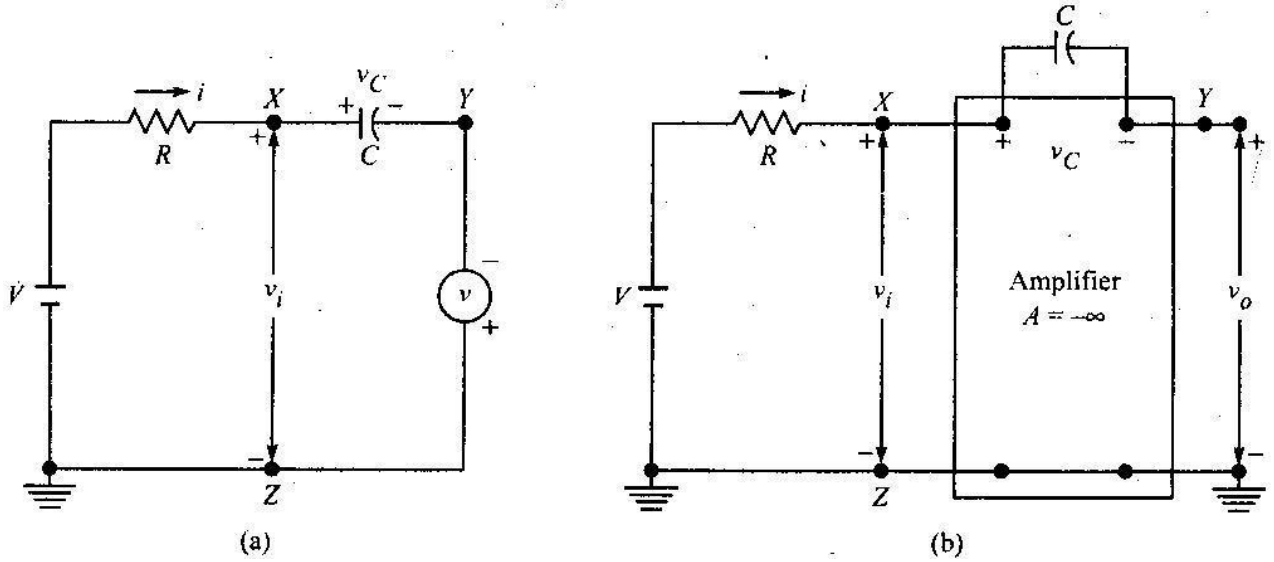


Fig. 5.4 (a) Figure 5.3(b) with Z grounded and (b) Miller integrator circuit.

the voltage between X and Z is equal to zero. Hence the point X acts as a virtual ground. Now for the amplifier, the input is zero volts and the output is a finite negative value. This can be achieved by using an operational integrator with a gain of infinity. This is normally referred to as the Miller integrator circuit or the Miller sweep. Suppose that the point Y in Figure 5.3(b) is grounded and the output is taken at Z. A linear sweep will appear between Z and ground and will increase in the positive direction. Let us now replace the fictitious generator by an amplifier with input terminals XY and output terminals ZY as shown in Figure 5.5. Since we have assumed that the generated voltage v at any instant is equal to the voltage across the capacitor vc, then *v0* must be equal to v,-, and the amplifier voltage gain must be equal to unity. The circuit of Figure 5.5 is referred to as the Bootstrap sweep circuit.

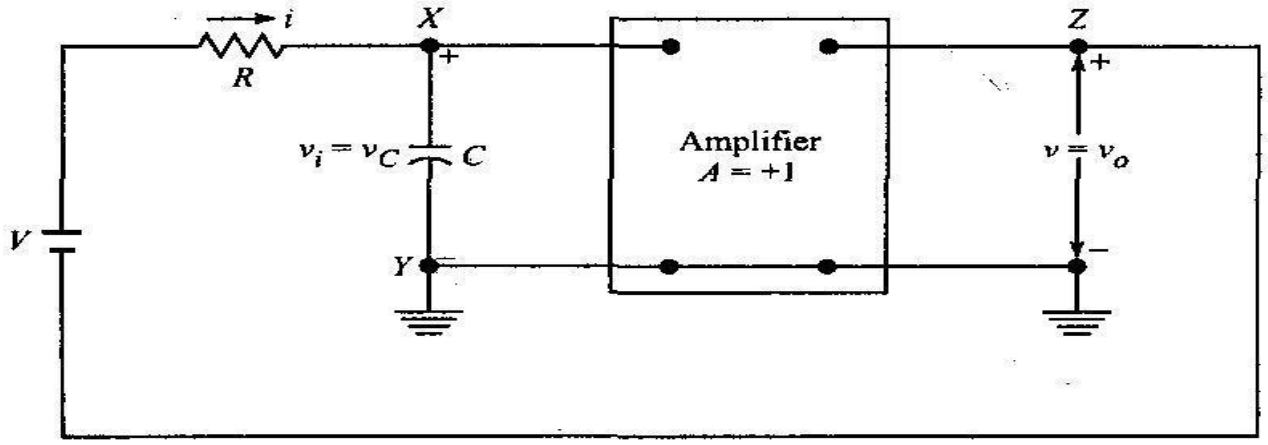


Fig. 5.5 Bootstrap sweep circuit.

The Miller sweep

The Miller integrating circuit of Figure 5.4 (b) is redrawn in Figure 5.6(a). A switch S at the closing of which the sweep starts is included. The basic amplifier has been replaced at the input side by its input resistance and on the output side by its Thevenin's equivalent. *R0* is the output resistance of the amplifier and *A* its open circuit voltage gain. Figure 5.6 (b) is obtained by replacing *V, R* and tf, on the input side by a voltage source *V* in series with a resistance *R'* where

$$V' = V\frac{R_i}{R_i + R} = \frac{V}{1 + \frac{R}{R_i}} \quad \text{and} \quad R' = R \| R_i = \frac{RR_i}{R + R_i}$$

Neglecting the output resistance in the circuit of Figure 5.6 {b), if the switch is closed at *t* = 0 and if the initial voltage across the capacitor is zero, then *v0* (f = 0+) = 0, because at / = 0~, V; ~ 0 and since the voltage across the capacitor cannot change instantaneously.

$$\text{At } t = 0^+, \qquad v_i - Av_i = 0 \qquad \text{or} \qquad v_i = Av_i = v_o = 0$$

This indicates that the sweep starts from zero.

At *t* = ∞, the capacitor acts as an open-circuit for dc. So no current flows and therefore

$$v_i = V' \qquad \text{and} \qquad v_o = AV'$$

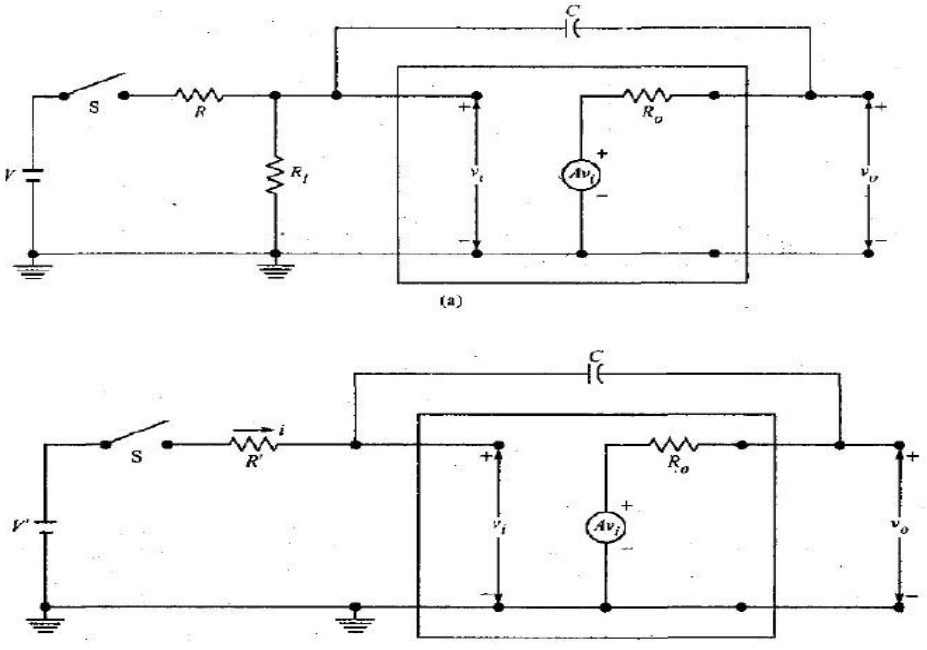


Fig. 5.6 (a) A Miller integrator with switch S, input resistance *Rf* and Thevenin's equivalent on the output side and (b) Figure 5.6(a) with input replaced by Thevenin's equivalent.

This indicates that the output is exponential and the sweep is negative-going since *A* is a negative number.

$$\text{Slope error, } e_s = \frac{V_s}{V}$$

where *Vs* is the sweep amplitude and *V* is the peak-to-peak value of the output

$$e_s(\text{miller}) = \frac{V_s}{|A|V'} = \frac{V_s}{|A|} \cdot \frac{R_i + R}{VR_i} = \frac{V_s}{V} \cdot \frac{1 + \dfrac{R}{R_i}}{|A|}$$

The deviation from linearity is $\dfrac{1 + \dfrac{R}{R_i}}{|A|}$ times that of an *RC* circuit charging directly from a source *V.* If *R0* is taken into account, the final value attained by *v0* remains as before, *AV* = - \A\V. The initial value however is slightly different.

To find *v0* at *t* = 0+ , writing the KVL around the mesh in Figure 5.13(b), assuming zero voltage across the capacitor, we have

$$V' - R'i - R_o i - Av_i = 0$$

$$v_i = V' - R'i$$

From the above equations, we find

$$v_i(t = 0^+) = \Delta v_i = v_o(t = 0^+) = \Delta v_o = \frac{\left(\dfrac{R_o}{R'}\right)V'}{1 - A + \dfrac{R_o}{R'}}$$

$$v_i(t = 0^+) \approx \frac{R_o V'}{R'|A|}$$

Therefore, if *R0* is taken into account, *v0(t* = 0+) is a small positive value and still it will be a negative going sweep with the same terminal value. Thus the negative-going ramp is preceded by a small positive jump. Usually this jump is/small compared to the excursion *AV',* Hence, improvement in linearity because of the increase in total excursion is negligible.

The bootstrap sweep

Figure 5.7 shows the bootstrap circuit of Figure 5.5. The switch S at the opening of which the sweep starts is in parallel with the capacitor *C.* Here, Ri,- is the input resistance, *A* is the open-circuit voltage gain, and *R0* is the output resistance of the amplifier.

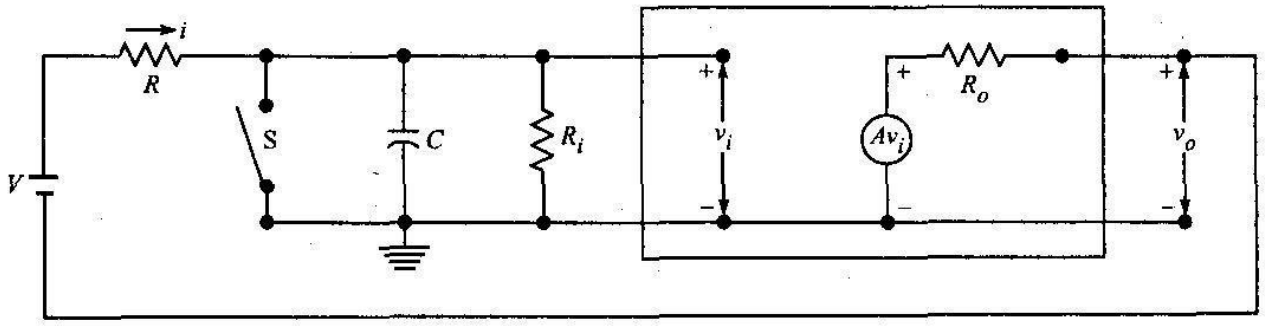


Fig. **5.7 Bootstrap** circuit of Figure 5.5 with switch S which opens at (= 0, input resistance *Rf,* and Thevenin's equivalent of the amplifier on the output side.

At *t* = 0~, the switch was closed and so *vt* - 0, Since the voltage across the capacitor cannot change instantaneously, at *t* = 0* also, v(- = 0 and hence Av, = 0, and the circuit shown in Figure 5.8 results.

$$t = 0^+, \qquad v_o = -V\frac{R_o}{R + R_o}$$

The output has the same value at *t* = 0 and hence there is no jump in the output voltage at *t* = 0.

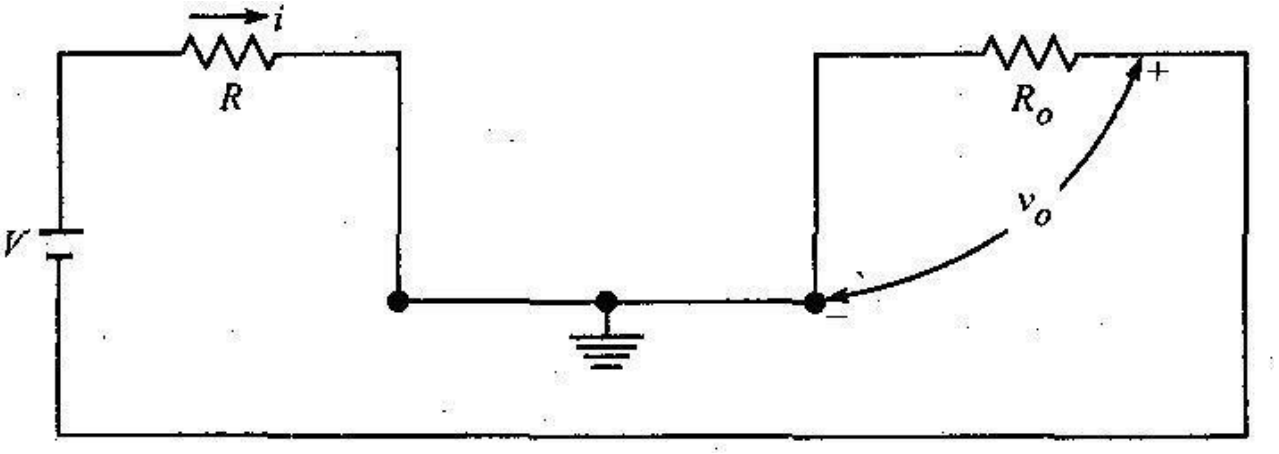


Fig.5.8 Equivalent circuit of Figure 5.7 aU = 0.

At *t* = ∞, the capacitor acts as an open-circuit and the equivalent circuit shown in Figure 5.9 results.

$$v_o(t = \infty) = AV_i - iR_o = AiR_i - iR_o = i(AR_i - R_o)$$

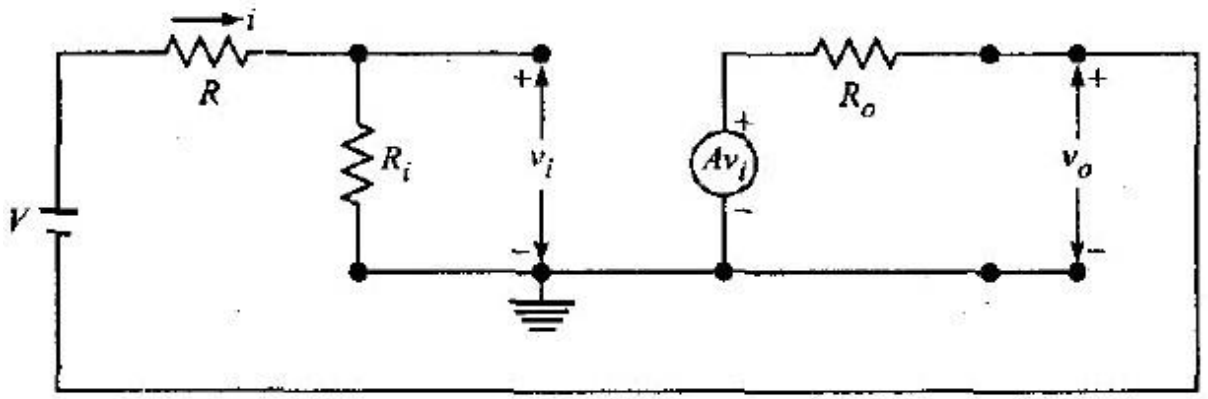


Fig 5.9 Equivalent circuit of Fig.5.7 at t= ∞

Writing KVL in the circuit of Figure 5.9,

$$V - iR - iR_i + AV_i - iR_o = 0$$

i.e.
$$i = \frac{V}{R + R_o + R_i(1 - A)}$$

$\therefore$
$$v_o(t = \infty) = \frac{V(AR_i - R_o)}{R + R_o + R_i(1 - A)}$$

Since *A* « 1, and if *R0* is neglected, we get

$$v_o(t = \infty) = \frac{V}{(1 - A) + \frac{R}{R_i}}$$

$$v_o(t = \infty) - v_o(t = 0) = \frac{V}{(1 - A) + \frac{R}{R_i}}$$

$$e_s(\text{bootstrap}) = \frac{\text{Sweep amplitude}}{\text{Total excursion of output}} = \frac{V_s}{V\left[(1 - A) + \frac{R}{R_i}\right]} = \frac{V_s}{V}\left(1 - A + \frac{R}{R_i}\right)$$

This shows that the slope error is [1 - *A* + *(R/Rj)]* times the slope error that would result if the capacitor is charged directly from *V* through a resistor.

Comparing the expressions for the slope error of Miller and bootstrap circuits, we can see that it is more important to keep *R/Rj* small in the bootstrap circuit than in the Miller circuit. Therefore, the Miller integrator has some advantage over the bootstrap circuit in that in the Miller circuit higher input impedance is less important.

THE TRANSISTOR MILLER TIME-BASE GENERATOR

Figure 5.10 shows the circuit diagram of a transistor Miller time-base generator. It consists of a three stage amplifier. To have better linearity, it is essential that a high input impedance amplifier be used for the Miller integrator circuit. Hence the first stage of the amplifier of Figure 5.10 is an emitter follower. The second stage is a common-emitter amplifier and it provides the necessary voltage amplification. The third stage (output stage) is also an emitter follower for two reasons. First, because of its low output impedance *R0* it can drive a load such as the horizontal amplifier. Second, because of its high input impedance it does not load the collector circuit of the second stage and hence the gain of the second stage can be very high. The capacitor C placed between the base of Qi and the emitter of Q3 is the timing capacitor. The sweep speed is changed from range to range by switching *R* and *C* and may be varied continuously by varying VBB.

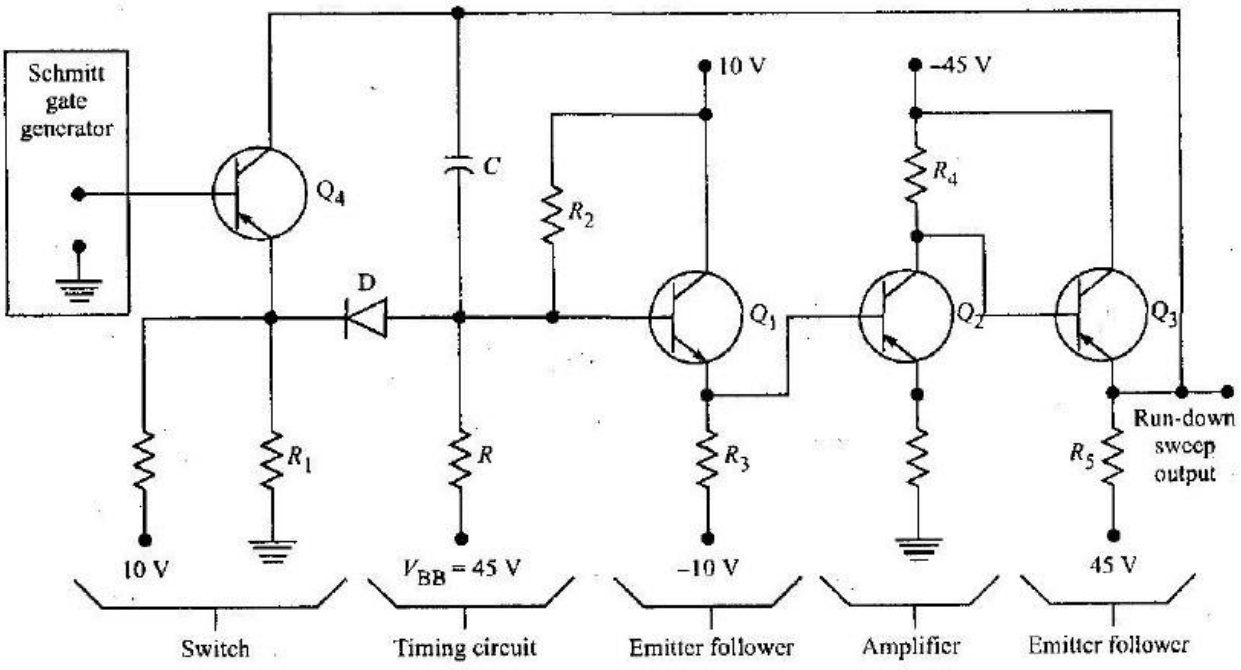


Fig.5.10 A Transistorized Miller Time-Base Generator

Under quiescent condition, the output of the Schmitt gate is at its lower level. So transistor Q4 is ON. The emitter current of Q4 flows through *RI* and hence the emitter is at a negative potential. Therefore the diode D conducts. The current through *R* flows through the diode D and the transistor Q4. The capacitor *C* is bypassed and hence is prevented from charging.

When a triggering signal is applied, the output of the Schmitt gate goes to its higher level. So the base voltage of Q4 rises and hence the transistor Q4 goes OFF. A current flows now from 10 V source through *RI.* The positive voltage at the emitter of Q4 now makes the diode D reverse biased. At this time the upper terminal of *C* is connected to the collector of Q4 which is in cut-off. The capacitor gets charged from VBB and hence a run down sweep output is obtained at the emitter of Q3. At the end of the sweep, the capacitor *C* discharges rapidly through D and Q4. Considering the effect of the capacitance *C*\, the slope or sweep speed error is given by

$$e_s = \frac{V_s}{V}\left(1 - A + \frac{R}{R_i} + \frac{C}{C_1}\right)$$

THE TRANSISTOR BOOTSTRAP TIME-BASE GENERATOR

Figure 5.11 shows a transistor bootstrap time-base generator. The input to transistor Q1 is the gating waveform from a monostable multivibrator (it could be a repetitive waveform like a square wave). Figure 5.12(a) shows the base voltage of Q1. Figure 5.12(b) shows the collector current waveform of Q1 and Figure 5.12(c) shows the output voltage waveform at the emitter of Q2

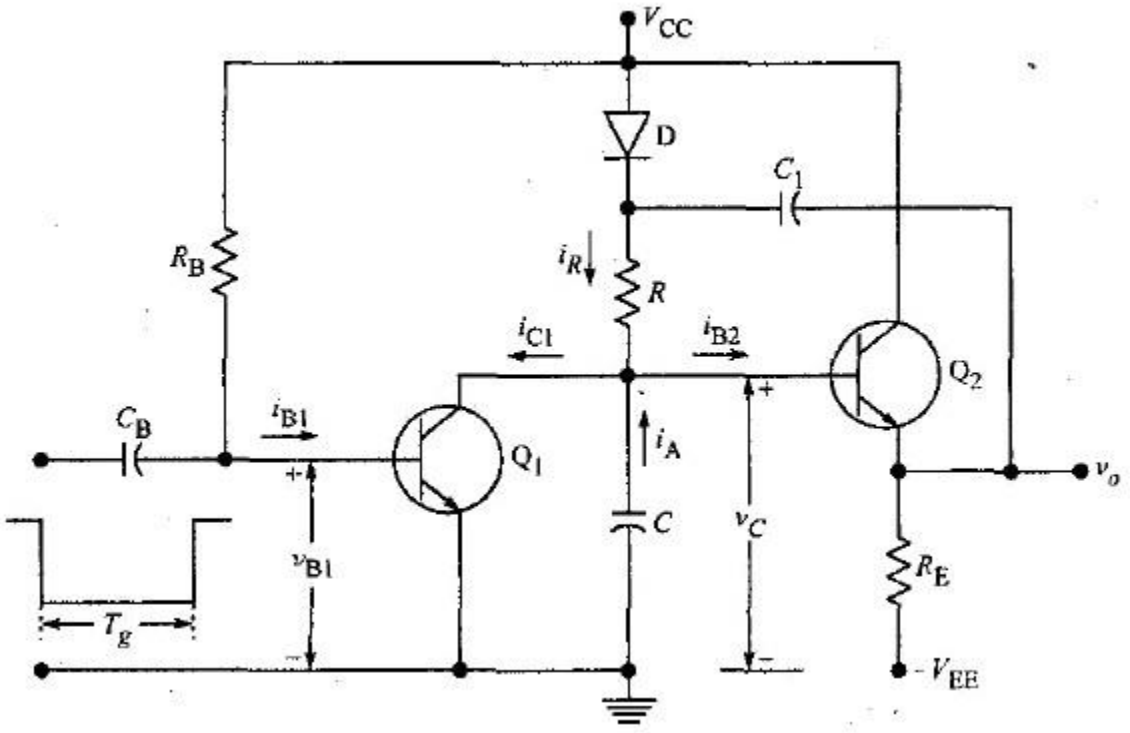


Fig.5.11 A Voltage Time Base Generator

Under quiescent conditions, i.e. before the application of the gating waveform at *t* - 0, Q| is in saturation because it gets enough base drive from *YCC* through ^B- So the voltage across the

capacitor which is also the voltage at the collector of Qj and the base of Q2 is VCE (sat). Since Q2 is conducting and acting as an emitter follower, the voltage at the emitter of Q2 which is also the output voltage is less than this base

voltage by VBE2, i.e. $v_o = V_{CE(sat)} - V_{BE2}$

is a small negative voltage (a few tenths of a volt negative). If we neglect this small voltage as well as the small drop across the diode D, then the voltage across *C*\ as well as across *R* is Vcc-Hence the current i> through *R* i§ *Vcc/R*- Since the quiescent output voltage at the emitter of Q2 is close to zero, the emitter current of Q2.

Hence the base current of Q2 is

iB2 = VEE /

hFE RE iR = iC1 + iB2

Since the base current of Q2, i.e. IB2 is very small compared with the collector current iC1 of Q1

$$i_{C1} \approx i_R \approx \frac{V_{CC}}{R}$$

For Q1 to be really in saturation under quiescent condition, its base current ((iB = *VCC/RB)* t be at least equal to 'IChFE> i.e. VCC//hFE^. so that

$$\frac{V_{CC}}{R_B} > \frac{V_{CC}}{h_{FE}R} \qquad \text{i.e.} \qquad R_B < h_{FE}R$$

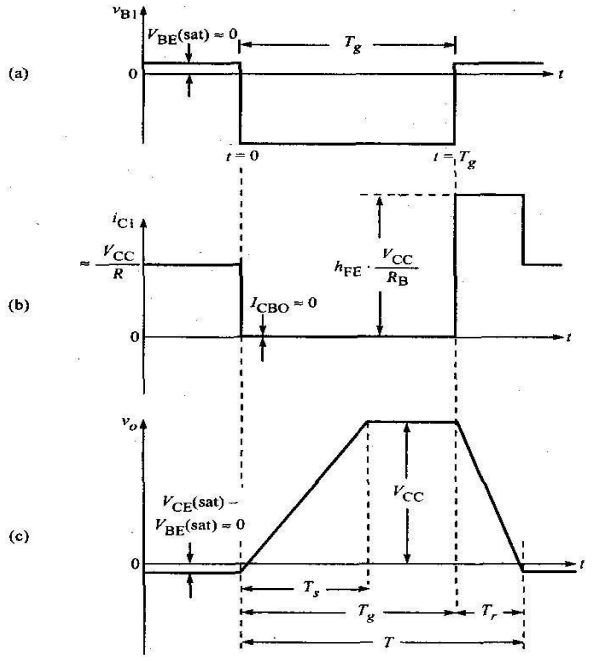


Fig.5.12 Voltage time-base generator of Figure 5.11: (a) the base voltage of Q1 (b) the collector current of Q1, and (c) the output voltage at the emitter of Q2

CURRENT TIME-BASE GENERATORS

We have mentioned earlier that a linear current time-base generator is one that provides an output current waveform a portion of which exhibits a linear variation with respect to time. This linearly varying current waveform can be generated by applying a linearly varying voltage waveform generated by a voltage time-base generator, across a resistor. Alternatively, a linearly varying current waveform can be generated by applying a constant voltage across an inductor. Linearly varying currents are required for magnetic deflection applications.

A SIMPLE CURRENT SWEEP

Figure 5.13 shows a simple transistor current sweep circuit. Here the transistor is used as a switch and the inductor *L* in series with the transistor is bridged across the supply voltage. *Rd* represents the sum of the diode forward resistance and the damping resistance. The gating waveform shown in Figure 5.26(b) applied to the base of the transistor is in two levels. These levels are selected such that when the input, is at the lower level the transistor is cut-off and when it is at the upper level the transistor Is in saturation. For $t < 0$, the input to the base is at its lower level (negative). So the transistor is cut-off. Hence no currents flow in the transistor and iL = 0 and VCE = Vcc- At f = 0, the gate signal goes to its upper level (positive). So the transistor conducts and goes into saturation. Hence the collector voltage falls to vCE(sat) and the entire supply voltage *Vcc* is applied across the inductor. So the current through the inductor

$$i_L = \frac{1}{L}\int V_{CC}\, dt = \frac{V_{CC}t}{L}$$

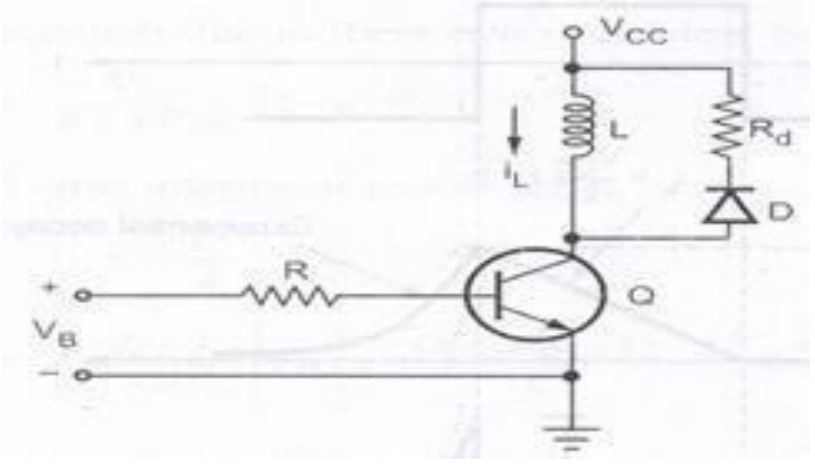


Fig.5.13 simple transistor current sweep circuit

Increases linearly with time. This continues till *t = Tg,* at which time the gating signal comes to its lower level and so the transistor will be cut-off. During the sweep interval *Ts* (i.e. from *t* = 0 to *t = Tg),* the diode D is reverse biased and hence it does not conduct. At *t ~ Ts,* when the transistor is cut-off and no current flows through it, since the current through the inductor cannot change instantaneously it flows through the diode and the diode conducts. Hence there will be a voltage drop of *lLRd* across the resistance *Rd.* So at *t = Tg,* the potential at the collector terminal rises abruptly to Vcc + *fiftd** ie - there is a voltage spike at the collector at *t = Tg.* The duration of the spike depends on the inductance of Z-^but the amplitude of the spike does not. For *t > Tg,* the inductor current decays exponentially to zero with a time constant *T- LIRd.* So the voltage at the collector also decays exponentially and settles at Vcc under steady-state conditions. The inductance *L* normally represents a physical yoke and its resistance *RL* may not be negligible. If *RCs* represents the collector saturation resistance of the transistor, the current increases in accordance with the equation

$$i_L = \frac{V_{CC}}{R_L + R_{CS}}(1 - e^{-(R_L+R_{CS})t/L})$$

$$\approx \frac{V_{CC}}{R_L + R_{CS}}\left(1 - \left\{1 - \frac{(R_L + R_{CS})t}{L} + \frac{1}{2}\left(-\frac{(R_L + R_{CS})t}{L}\right)^2\right\} + \dots\right)$$

$$= \frac{V_{CC}t}{L}\left(1 - \frac{1}{2}\frac{(R_L + R_{CS})t}{L}\right)$$

If the current increases linearly to a maximum value *IL,* the slope error is given by

$$e_s = \frac{I_L}{\frac{V_{CC}}{R_L + R_{CS}}} = \frac{(R_L + R_{CS})I_L}{V_{CC}}$$

A TRANSISTOR CURRENT TIME-BASE GENERATOR

Figure 5.14 shows the circuit diagram of a transistor current time-base generator. Transistor Q1 is a switch which serves the function of S . Transistor Q1 gets enough base drive from VCC1 through KB a °d hence is in saturation under quiescent conditions. At t = 0, when the gating signal is applied it turns off Q1 and a trapezoidal voltage waveform appears at the base of Q2. Transistors Q2 and Q3 are connected as darlington pair to increase the input impedance so that the trapezoidal waveform source is not loaded. Such loading would cause nonlinearity in the ramp part of the trapezoid. The emitter resistor *RE* introduces negative current feedback into the output stage and thereby improves the linearity with which the collector current responds to the base voltage. For best linearity it is necessary to make the emitter resistance as large as possible. *RE* is selected so that the voltage developed across it will be comparable to the supply voltage

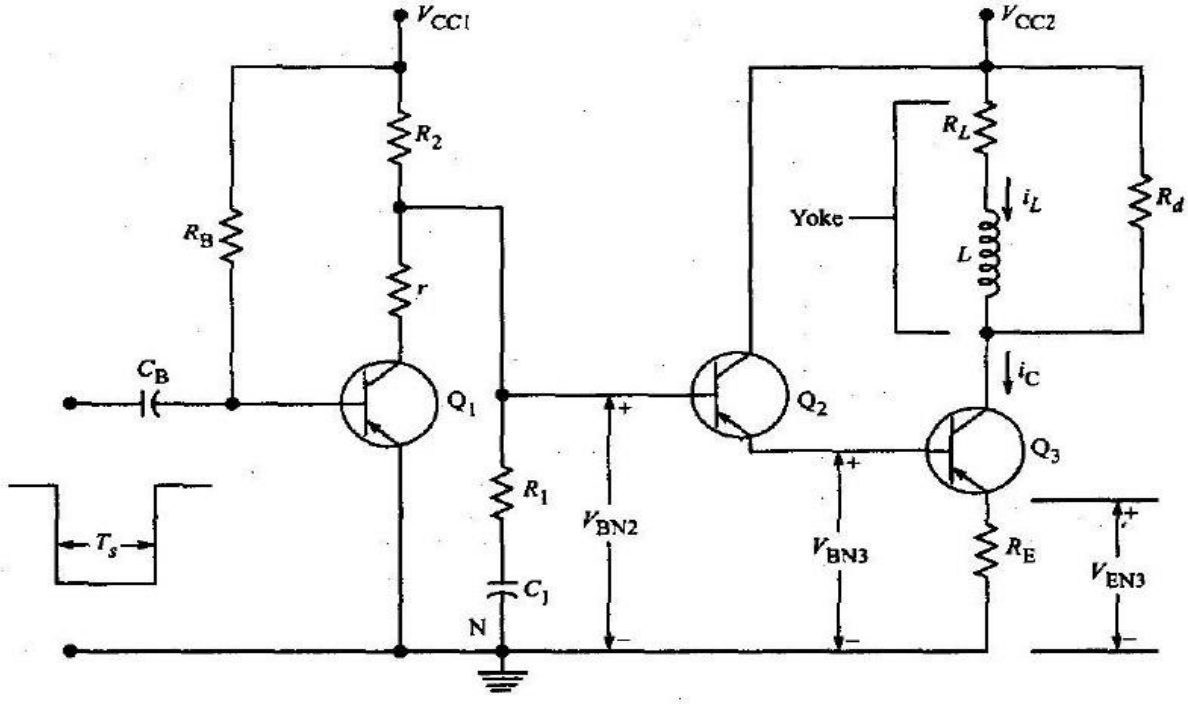


Fig.5.14 A Transistor Current Sweep Circuit

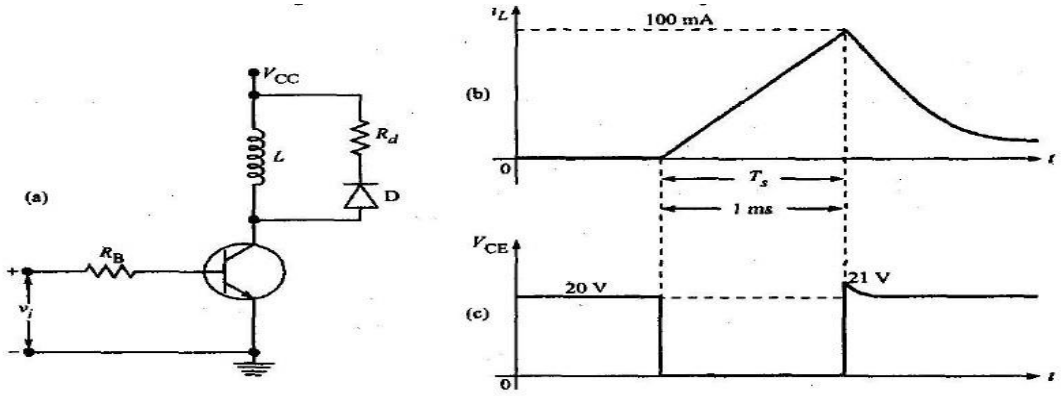


Fig.5.14 a) Circuit Diagram b) waveform of iL c)waveform of VCE